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RECENT DEVELOPMENT OF RAPID SINGLE FLUX QUANTUM (RSFQ) LOGIC DIGITAL DEVICES

O.A.Mukhanov†, S.V.Rylov‡, V.K.Semenov‡, and S.V.Vyshenskii†

†Institute of Nuclear Physics, and ‡Department of Physics,
Moscow State University, Moscow, 119899 GSP, U.S.S.R.

The RSFQ logic family is proved to be naturally suitable for asynchronous self-timed Josephson computational structures. This assessment is discussed on apparent examples of non-recursive and recursive devices with operating frequency of up to 100 GHz (for state-of-the-art Nb Josephson technology) irrespective of their complexity.

I. Introduction

The main progress in Josephson junction digital technologies was achieved with latching logic elements (1). These elements, however, do have a principle drawback - the necessity of the whole system reset procedure by means of the ac current supply. Hence the upper clock frequency limit of 1 GHz (already crossed by fast semiconductor devices).

It has been shown that the basic elements of the recently proposed RSFQ logic family (its main attributes are compiled in Tables 1-3) can operate at extremely high clock frequencies - from 30-50 GHz for 10-μm Nb technology, and up to 500 GHz for 1-μm Nb technology. These results of numerical simulations (2, 3) have already gained confirmation in experiments with single one-bit elements implemented in 10-μm and 5-μm design rules technology (4-6).

Table 1.* The main features of the RSFQ logic family.

Name	Delay δ_L/τ_0	Complexity N	Bias i_b/i_c	Area¶ A/λ^2
Interconnecting elements (without memory)				
A stage of JDTL	1+	1	0.7	100/ 30
Unidirectional (plain) buffer	1	2	1	210/ 60
Split buffer	1	1	1	140/ 50
Confluence element	2	5	3.2	570/180
dc/SFQ converter	-	2	-	220/ 70
"Non-logic" elements or asynchronous flip-flops				
Coincidence junction	2	3	1.4	350/110
T flip-flop	1	4	1.4	480/150
"Logic" elements or clocked flip-flops				
D flip-flop	2	4	1.5	480/150
Inverter	3	5	1.4	580/170
D flip-flop w/NDRO	2	6	2	680/220
SFQ/dc converter	-	6	4.7	680/220
2-input OR	3	9	3.8	930/290
Exclusive OR	3	9	2.4	1000/300
1-bit full-adder	8	22	9.6	2500/830

+ - This line stage can serve as a delay adjustable by a special resistor shunting a Josephson junction.

With such rapid elements it is necessary to use specific design technique meant to increase device operational frequency up to that of elements and to make it irrespective of the device complexity. This problem was successfully settled in Ref. (7) for both serial and parallel arithmetic blocks by means of the asynchronous bit-level communications of basic gates.

Moreover, in the same paper a general approach to design of the RSFQ logic based devices was presented. Its essence is a consistent transfer of well known pipeline and self-timing techniques to one-bit-processing level with hard employment of the intrinsic memory inherent to each "logic" RSFQ element. This feature upgrades these elements to substantially reacher class of clocked flip-flops rather than mere logic gates.

The main goal of the present paper is to demonstrate rich abilities of this approach on more general set of examples.

Table 2.* Natural time and voltage units

λ, μm	10	5	2.5	1
τ_0, ps	7	4	2	1
V_b, mV	1.2	2	4	8

Table 3.* Natural current units

T_W, K	4.2	8	25	77
i_c, mA	0.1	0.2	0.6	2

* - τ_0 - characteristic duration of single flux quantum transition of underbiased overdamped ($\beta_c \approx 1$) Josephson junction; δ_L - minimal logic delay of an element; λ - design rules of Josephson junction Nb technology; i_b - bias current of the whole element, supplied by the common dc voltage source V_b through the appropriate resistors; i_c - minimal critical current of a junction, ensuring the stability with respect to thermal fluctuations at working temperature T_W; N - number of Josephson junctions in the element

¶ - A - area, consumed by the element in two Nb technologies. First number - from Ref. (6), second number - estimation for $J_c \approx 10^5$ A/cm^2.

II. Essentials of the RSFQ logic circuitry

A. Clocked flip-flops as "logic" elements. The most primitive RSFQ element is the D flip-flop cell (3) shown in Fig. 1. It contains two-junction interferometer with two steady states ("0" and "1"). The states are switched by SFQ voltage pulses V(t):

$$\int V(t)dt \le \Phi_0 \qquad (1)$$

that come through the inputs X and T. Besides the pulse T may cause output SFQ pulse Y (on the junction J_2).

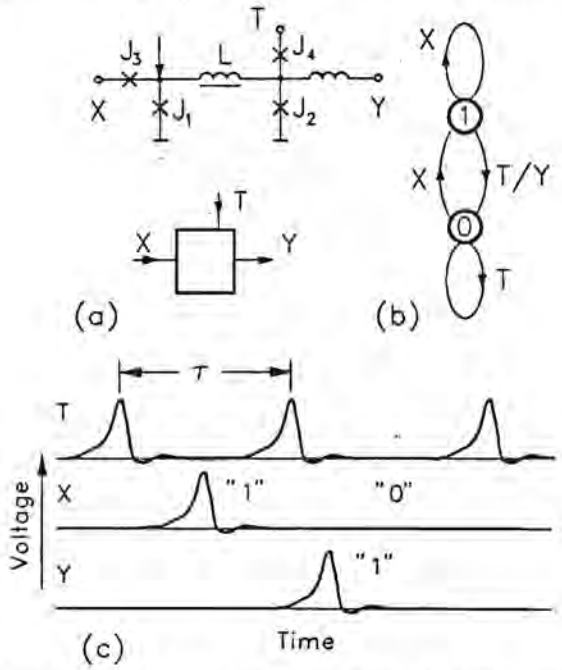

Fig. 1. D flip-flop as simplest "logic" RSFQ element: (a) notation and equivalent circuit; (b) diagram of state transitions induced by SFQ input pulses X and T. One followed by the output is marked with /Y; (c) time diagram.

State transition diagram and time diagrams (Fig. 1b, c) apparently demonstrate the similarity of this D cell with asynchronous R-S flip-flop. The only distinction 's the way of information presentation – in a form of picosecond pulses (see Eq. 1) rather than dc voltage. Hence this cell may be used as clocked D flip-flop provided input T is fed with timing pulses. Really, D flip-flop cell (Fig. 1) logs the fact of the arrival ("1") or non-arrival ("0") of data pulses X in between the two consequent (timing) pulses T. The latter one produces appropriate output signal Y in the form of presence ("1") or absence ("0") of the SFQ pulse. The cell contains only four Josephson junctions (equivalent in complexity to four p-n junctions or two transistors), whereas performs the function of a clocked flip-flop.

All "logic" RSFQ elements are in fact clocked flip-flops. Some of them perform simple functions of well known primitive flip-flops. For instance RSFQ inverter element (3) is a mere D flip-flop with inverse output. Others have highly complicated functional specifications.

For example "exclusive OR" RSFQ element (Fig. 2) includes two storage interferometers and can reside in three states – without flux quanta (initial "00" state) and with a single quantum in one of the interferometers ("01" and "10" states).

In the examples mentioned above the timing pulse always performed the destructive read out (DRO), i.e. two operations simultaneously – the data read out and the reset of the element. These actions may be separated (7), so to perform non-destructive data read out (NDRO) without alteration of the flip-flop state. With this sort of elements one can transform data from SFQ representation to common dc one and vise versa (6).

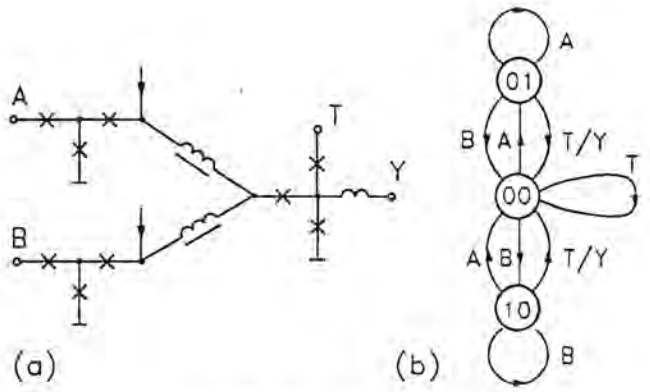

Fig. 2. Exclusive OR clocked flip-flop: (a) equivalent circuit; (b) diagram of state transitions induced by input pulses A, B and T. Ones followed by the output is marked with /Y.

Asynchronous flip-flops. The main RSFQ element for timing signals processing is coincidence junction or Müller C-element (7) (Fig. 3). Input pulses for coincidence junction are to arrive in pairs, though with arbitrary mutual delay. The last pulse in each pair causes the generation of the output pulse and the reset of the element. Another example of asynchronous flip-flop is a well known binary counter (6,8). Note a small delay (2-3 τ_0) of one-bit operation.

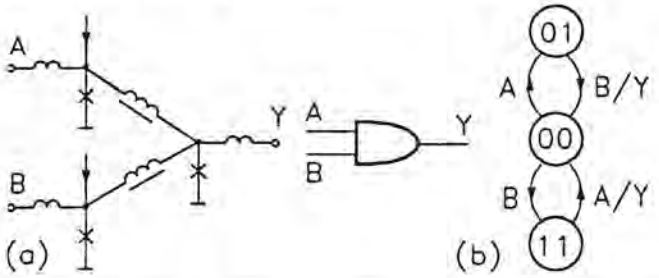

Fig. 3. Coincidence junction or Müller C-element: (a) notation and equivalent circuit; (b) diagram of state transitions induced by SFQ input pulses A and B.

Interconnecting elements. The interconnection of the RSFQ elements is executed by buffers containing at least one stage of Josephson discrete transmission line (JDTL) (Fig. 4a) wasting τ_0 delay per stage (10).

Split buffer (Fig. 4b) is a direct analog of a previous one. It differs by extra inductance and parameters of Josephson junction. Split and plain buffers may be mixed if (and as) needed.

Our confluence ("wired OR") element (Fig. 4c) comprises five Josephson junctions. It unidirectionally passes SFQ pulses from two inputs to an output.

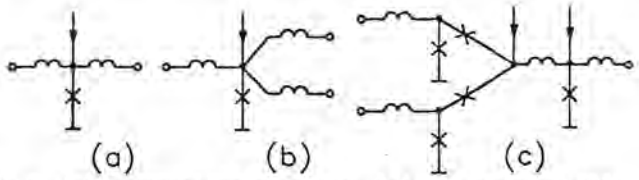

Fig. 4. Interconnecting elements: (a) one stage of JDTL; (b) split buffer; (c) confluence buffer.

III. Primitive shift structures

Asynchronous shift structure. The simplest structure for asynchronous pipelined data transfer is a chain of cells D (Fig. 5a), linked via interconnecting elements. The timing pulse T arriving from the right inspires read out of data bit stored in the rightmost cell (with concurrent reset of the cell). The same pulse T delayed by Δ approaches the next cell and starts the carry of data bit that have been stored in it to the (now empty) rightmost cell. This process of an empty cell carry continues until the pulse T runs through the entire structure, provided

$$\Delta > \delta_L , \quad \tau > \delta_L , \qquad (2)$$

where Δ is the minimal delay between arrival of pulse T to neighboring cells, and τ - minimal time period between two consequent pulses T.

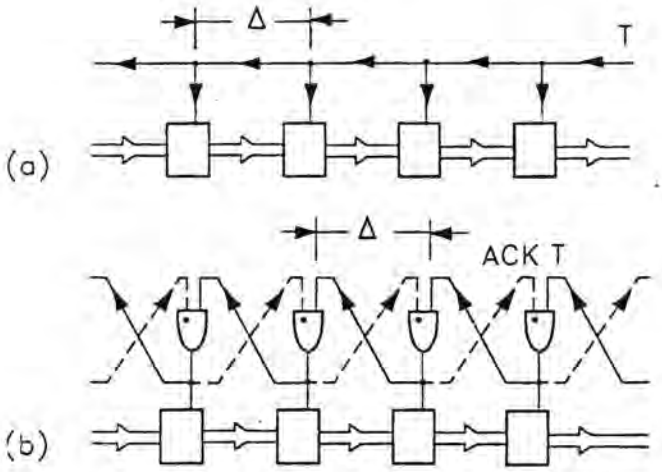

Fig.5. Simplest data shift structures: (a) externally clocked shift register; (b) self-timed shift register.

The relations (Eq. 2) show that our shift structure is substantially distributed; during τ period the computational activity wave front may travel for only one space period of the structure.

The obvious drawback of such a "non-respondent" data exchange algorithm is the absence of the recipient readiness acknowledgement signal ACK.

Self-timed shift structure. The simplest self-timed structure employing a full hand-shaking data exchange algorithm (11) is shown on Fig. 5b. It differs from the former one by the presence of coincidence junctions that should be trespassed by the timing pulses coming to every cell. These junctions are preset to the "10" state by pre-feeding the dot-marked inputs.

Thus the first pulse T may pass through the whole structure (just like in the previous case on Fig. 5a) and activate all the cells D successively with relative delay Δ. The same pulse T resets each coincidence junction to the "closed" "00" state. And the pass of the next pulse T becomes possible only after arrival (through the special line dashed on Fig. 5b) of ACK signal, that "opens" the coincidence junction.

The minimal period τ is set by the sum of T and ACK pulses transfer times between the nearest cells:

$$\tau > \Delta + \delta_{ACK}, \qquad (3)$$

rather than by the clock generator.

Second, the feedback is established between the data source and the receiver, so that the T pulses generation would be suspended as soon as data consumer is busy.

IV. Buffered shift structures

Rather a rigid constraint (Eq. 2) on the speed of computational activity wave front may be removed with the help of additional D flip-flop buffer cells. Moreover, the direction of computational activity wave front propagation may be made entirely independent of the direction of data flow.

Data counter timing flow. As is seen from Fig. 6a, the first timing pulse successively passes through all (now "open") coincidence junctions of the shift structure and initially induces the data transfer from underneath cells to the neighboring (now empty) buffer cells E. The events of activating different cells are now independent of data events and delays. Thus the minimal propagation delay Δ of the computational activity wave front becomes unrelated with the time period δ_L of data processing: $\Delta > 0$.

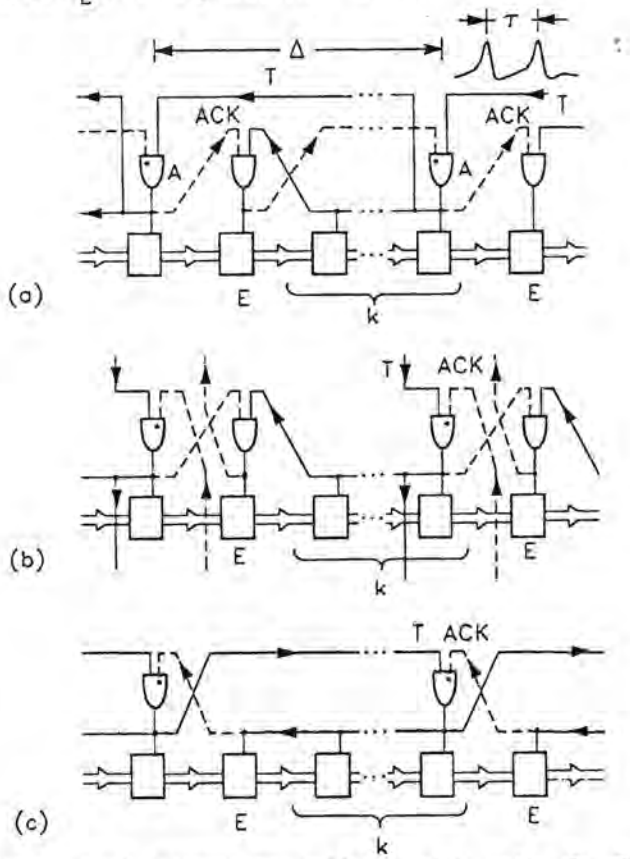

Fig.6. Shift structures buffered with cells E. The timing (T) pulses flow: (a) counter; (b) across and (c) along the data (——) pulses.

Then an empty cell begins to "drift" to the left along the short k-cell chain. But the (k+1)-th (i.e. E) cell will be emptied only after the arrival of the ACK pulse at the coincidence junction B above cell E. While activating the cell E, junction B "opens" the main coincidence junction A for the next pulse T. Hence

$$\tau \geq (k+1)\ \delta_L . \qquad (4)$$

Data across timing flow. Fig. 6b shows slightly modified shift structure that tolerates not only arbitrary period Δ, but also arbitrary order of pulses T arrival at the neighboring cells: $\Delta \lesssim 0$. Thus this structure allows for the perpendicular propagation of computational activity wave front and that of data.

Data along timing flow. And finally, the structure for parallel timing pulses and data shift is shown on Fig. 6c. Here the speed of computational activity front is also not limited by the logic delays of the cells.

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V. Simplest recursive devices

Look-ahead N-cell FIFO register. The shift structures considered above when used as FIFO registers provide overall delay proportional to the length N of a structure. Fig. 7 shows another type of FIFO register with overall delay independent of N. It incorporates two more simple shift structures (of the length N/2) - one with data along and another with data counter timing flow. Data and timing terminals of both parts are linked (may be via coincidence junctions). For k=1 (Cf. Eq. 4) overall cycle τ is only twice the timing cycle of a single primitive cell D. With its output and input wired together the FIFO register forms the simplest recursive device - sequential access memory.

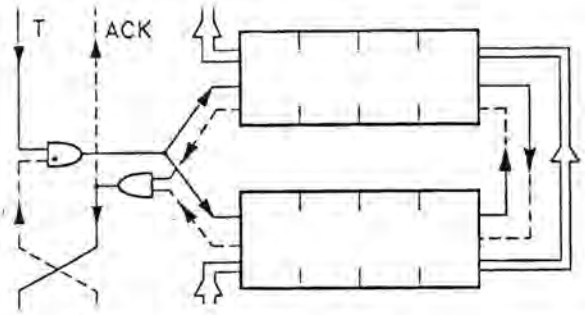

Fig.7. N-cell FIFO register contains two shift registers - one with timing flow along, and one counter data flow.

Controller for serial RSFQ arithmetic chip (Fig. 8). Being fed with initializing pulse INIT the controller should issue the first pulse T. Then each ACK pulse provokes the next pulse T, etc. After issuing previously specified number of pulses T, our controller should signalize (READY) the termination of its activity and wait for the next INIT.

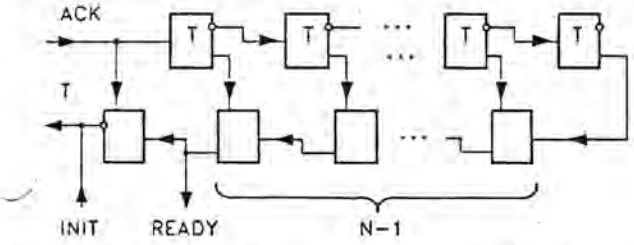

Fig.8. Controller. T - asynchronous T flip-flop; the leftmost cell is RSFQ inverter.

The heart of the controller is a usual binary counter (6, 8), shown in the upper part of the Fig. 8, that counts ACK pulses. It is enhanced so to produce overflow signal within δ_L delay upon the arrival of the last ACK pulse. That is why one of aforementioned shift structures is attached (as a lower part of Fig. 8) to the counter. The timing and input data signals for this structure come from the counter cells.

When the counter comes to the state "11...11", the inverter is fed by "1" signal. The nearest ACK pulse resets the counter and at the same moment ceases the generation of "1" (in fact T) pulses on the output of the inverter and of the whole controller.

V. Discussion

The considered set of RSFQ devices is perfectly suitable for experimental study. Shift structures are the recognized touchstone for all new circuit design techniques (9, 10) and thus are especially convenient for their comparison.

One can readily build numerous useful devices with our tool kit. We mention just adjustable digital delay for time domain reflectometer (11) and sequential access memory (they comprise the clock controller shown on Fig. 8 and N-cell FIFO register shown on Fig. 7).

Our main result is the demonstration of the fact that quite complicated devices of both non-recursive and recursive types can be assembled from our self-timed RSFQ circuitry. Timing rate of the whole device does not depend on its complexity and can be made as high as 100 GHz for the present day technology.

Our technique resembles Wavefront Array Processing (12) but instead of the whole processor chips as processing elements we employ blocks as tiny as one-bit gates. Besides we thoroughly explore the (usual here) "read out" feature of the timing pulse - the same timing pulse can be used later as acknowledgement signal. This gives the opportunity to escape the familiar verbose implementation of the data-driven communication algorithms (13) of self-timed systems.

Our treatment demonstrates the fruitfulness of the multi chip system organizational discipline transfer to the RSFQ chip level, and makes quite challenging the possibility of a similar transfer from local area nets domain to the RSFQ multi chip level.

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