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RECENT RESULTS IN RSFQ DIGITAL APPLICATIONS

O. MUKHANOV, P. BRADLEY, D. GAIDARENKO, D. GUPTA, S. KAPLAN, A. KIRICHENKO, S. RYLOV, and E. TRACK
HYPRES, Inc. 175 Clearbrook Road, Elmsford, NY 10523, USA

ABSTRACT

Design and test results are discussed towards the development of the first superconductive digital applications - signal and time digitizers. HYPRES is developing a 6 effective bit, 10 GHz transient digitizer with 20 GHz demultiplexers, a 18 effective bit, 10 MHz high-resolution signal digitizer, and a 12 ps multi-hit time digitizer.

INTRODUCTION

Out of a great variety of digital applications, we have been pursuing several digital circuits with the best chances for commercial success in the nearest future. We use three criteria to assess circuits capable of competing with the multi-billion semiconductor technology. First, the circuits performance specifications must be beyond the reach of semiconductor circuits. Second, the integrated circuit complexity should be within existing capabilities of superconductor circuit fabrication. In practical terms, these circuits should have a complexity level of a few thousand Josephson junctions, readily available today at HYPRES' low-temperature superconductor (LTS) foundry [1]. Third, the circuits' input/output (I/O) requirements should not exceed the level of interface technology available today or in the nearest future. The interface capabilities can be quantified by the aggregate data rate, which is limited now at approximately 160 Gb/s (e.g. 64 lines at 2.5 Gb/s).

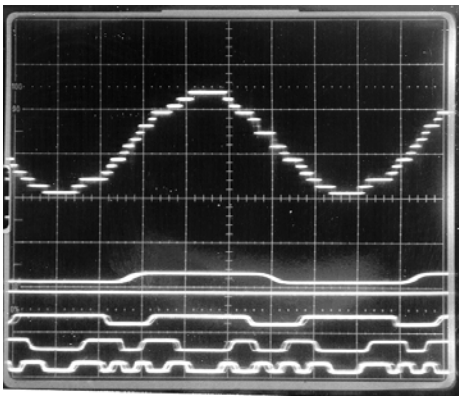
Superconductive digitizers for analog and time information conversion to digital form and processing are the focus of HYPRES' digital application efforts. They combine high performance, relatively low integrated circuit complexity, and realistic interface requirements. HYPRES is developing digitizers based on the flash analog-to-digital converters (ADCs) for fast instrumentation, high-resolution ADCs for radars, and time-to-digital converters (TDCs) for high-energy physics instrumentation. In all these applications, the superior performance is enabled by exploiting the unique set of fundamental properties of superconductivity unmatched by any other integrated circuit technology. These properties are short gate-switching time (1-2 ps) even for a 2 μm linewidth which scales linearly with linewidth and very low power dissipation (~1 microwatt per gate). Coherent electrons in a superconducting loop produce interference fringes analogous to those seen with lasers, but faster and with greater sensitivity. This property enables periodic behavior with fundamental accuracy - the key to a high performance digitization. Extremely low noise at liquid helium temperature (4K) is another important advantage of superconductive digitizers. All our circuits are based on RSFQ LTS technology. This enables easy integration of analog high-sensitivity RF front-end devices with digital post-processing and memory circuitry on a single chip, without straining the limits of speed and power dissipation, and mixed signal interference problems plaguing semiconductor digitizers. In this paper, we will present the latest results in the development of our digitizers based on flash ADC, high-resolution ADC, and TDC.

FLASH ADC

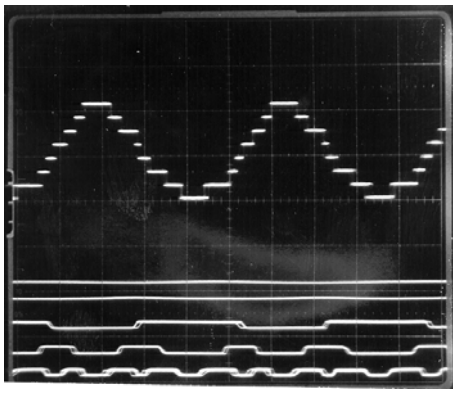
The superconductive flash ADC is capable of continuous digitization of analog signals with bandwidth in excess of 10 GHz. This new ADC design is an improvement over our older flash ADC design which had demonstrated 4 effective bits at 4 GHz input signal [2]. The goal now is to improve that performance and produce a 20 GS/s, 10-bit ADC with 6 effective bits at 10 GHz using the existing HYPRES fabrication process. In order to achieve this goal, we have changed our comparator design to a new RSFQ design capable of achieving ~0.5 ps threshold accuracy and have introduced a new architecture in which comparator outputs are being processed by RSFQ logic stages. The new 10-bit flash ADC contains 8 interleaved comparators to synthesize 4 least significant bits (LSBs), and 12 redundant comparators to generate the 6 most significant bits (MSBs) [3].

We have successfully demonstrated a considerable improvement in performance of the new RSFQ comparators using the 5-bit Gray-coded diagnostic ADC. The beat frequency tests performed demonstrate 5 effective bits at 4 GHz, 4 effective bits at 12 GHz, and 3 effective bits at 20 GHz (Fig. 1). They demonstrate full threshold width of 1 ps (0.4 ps rms jitter). Comparator dynamic range adequate for 9 effective bits at low speed signal has also been demonstrated. The individual comparators have been operating up to 40 GHz.

The implementation of the interleaved ADC section will enhance the resolution further by XOR-ing eight identical comparators with mutually shifted thresholds to synthesize three more effective bits. We are implementing a digital error correction scheme for the MSB section to fix most of the errors observed in Fig. 1. RSFQ look-back error correction circuits [4] are capable of correcting errors up to 1/8 of the comparator periodicity. We have successfully demonstrated a complete interleaved section synthesizing 4 LSBs. All circuit elements (multiplexers and shift registers) needed for full digital error correction have been separately demonstrated.



12.000001 GHz Signal
12.000000 GHz Clock



19.999995 GHz Signal
20.000000 GHz Clock

Fig. 1 Beat frequency tests above 10 GHz: reconstructed 12 and 20 GHz sinewaves and 5-bit ADC output. The right photo not only shows 20 GHz signal response, but demonstrates 20 GHz clocking for the ADC. Interleaving will produce even higher resolution.

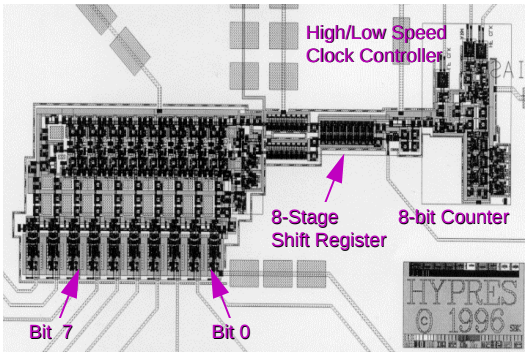


Fig. 2 Layout of a 1:8 RSFQ demultiplexer with diagnostic input shift register and clock controller. This circuit was successfully operated at 20 GHz.

The full-performance flash ADC will produce 8-bit output data at 20 GS/s, i.e. a 160 Gb/s aggregate data rate. In order to handle this data, we plan either to capture a part of the data on chip using the acquisition shift register memory or directly transport all data to room temperature electronics using RSFQ demultiplexers. RSFQ acquisition shift registers are well developed and successfully operated in acquisition mode up to 20 GHz [5]. However, the total capacity of this memory cannot be larger than 2-4 kbit (256-512 words x 8 bits) limited by the existing level of circuit integration. By demultiplexing the ADC outputs, we can overcome this problem and provide all data in real time.

We have developed a 1:8 demultiplexer using shift-and-dump architecture [6]. The optimized version of the demux based on the use of destructive readout cells to store and shift data [4] has been demonstrated up to 20 GHz with wide dc bias margin (±19%). Fig. 2 shows layout of the 1:8 demultiplexer integrated with clock-controlled test shift registers [7] to pre-load input data. The fully demultiplexed ADC approach will require the development of a 64-channel, 2.5 Gb/s interface which is under construction now. High-speed semiconductor amplifiers will sense and translate the pre-amplified RSFQ outputs of the demultiplexer to ECL levels. The pre-amplification from 0.3 mV to 3 mV will be performed by on-chip dc-driven drivers [7].

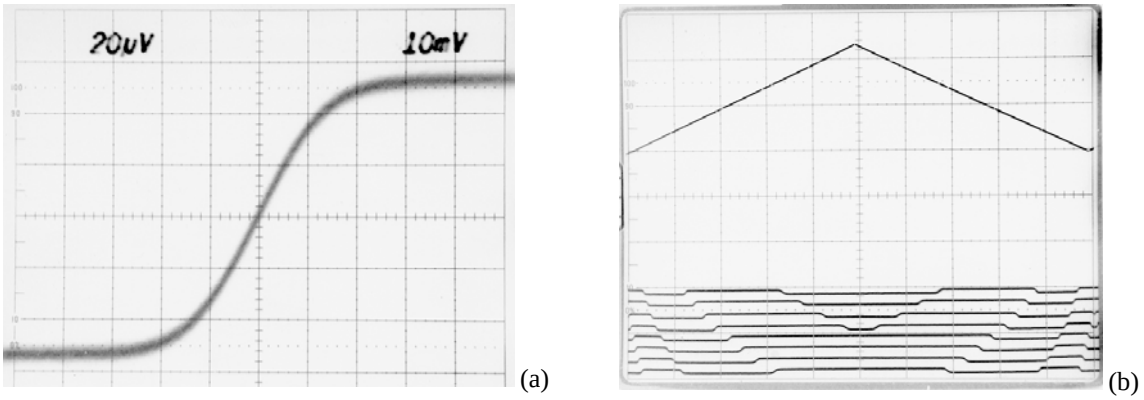
HIGH RESOLUTION ADC

The superconductive high-resolution ADC is optimized to digitize analog signals with bandwidth below 1 GHz. The goal is to build a 20 MS/s, 20-bit ADC with 18 effective bits at 10 MHz signal using the existing HYPRES fabrication process. HYPRES will achieve this goal by implementing a differential-code architecture based on a phase modulation-demodulation technique [8]. The phase modulator stage is a highly linear single-junction interferometer converting the analog input signal into delay-modulated SFQ pulses. The phase demodulator stage is a bank of interleaved race arbiters followed by a digital encoder to produce a differential code of the signal. The last stage of the ADC is a decimation digital filter to perform integration and filtering. The high performance of this architecture relies on a high-speed internal clock (above 10 GHz) and on the absence of any feedback loops. The whole ADC is essentially a straight, high-throughput, bit-pipelined circuit - the most favorable structure for RSFQ implementation. The strongest feature of this architecture is the ability to dynamically program performance with a bits-for-bandwidth tradeoff of 1.5 bits per octave (Table I) by setting the filter decimation ratio.

BW, MHz	f_{OUT}, *MS/s*	N=8, f_{CLK}=10 GHz	N=16, f_{CLK}=20 GHz	N=64*, f_{CLK}=40 GHz
80	160	11.4	13.9	17.4
40	80	12.9	15.4	18.9
20	40	14.4	16.9	20.4
10	20	15.9	18.4	21.9

** Requires transition from current 2.5 μm to 1 μm fabrication technology*

Table I. ADC performance tradeoffs: ADC resolution in effective bits as a function of number of interleaved arbiters N, bandwidth BW, and sampling rate f_{OUT} ($BW = f_{OUT}/2$).



(a) (b)

Fig. 3 High-speed operation of a 8-channel race arbiter at 20 GHz. (a) Time discrimination curve at 20 GS/s displaying threshold width of 3 ps (Horizontal scale is 1 ps/div). (b) Uniform interleaving of 8 channels at 17.5 GS/s. Top trace - input signal, bottom traces - output bits 1 to 8 of the race arbiter.

We have successfully demonstrated the phase modulator with an 8-channel race arbiter up to 20 GHz. The high-speed test results of an 8-channel race arbiter (Fig. 3) demonstrate that full transition width is 2 ps from dc to 15 GHz and 3 ps at 20 GHz. This is sufficient to build a 16-channel, 20 GHz race arbiter enabling a 20-bit, 20 MS/s ADC with 18 effective bits. The 10 GHz digital decimation filter has been designed based on a similar filter recently demonstrated at 10 GHz at SUNY, Stony Brook. To verify the ADC architecture, the smaller version has been fully integrated and demonstrated excellent linearity of 16 bits and 108 dB spurious-free dynamic range (SFDR).

The full-performance high-resolution ADC will produce maximum a 3-4 Gb/s aggregate data rate which is well within existing interface capabilities. HYPRES has already built an 18-channel, 20 Ms/s interface system to transport output digital data to a PC with a standard 50 MS/s logic analyzer card [9]. For operating the ADC at higher sampling rates, we are building a 200 MS/s VME bus compatible interface system.

TDC

The superconductive TDC is designed to measure the timing of events in high-energy and nuclear physics experiments [10]. There are two main advantages of a superconductive TDC which are beyond the reach of semiconductor counterparts. First, the very low power dissipation enables mating of the cooled sensors and TDC electronics. This eliminates cable bandwidth limitations. Second, unlike semiconductor TDCs, the multi-hit time resolution of the superconductive TDC is comparable with its time resolution. This allows the resolution of multiple physics events with high accuracy.

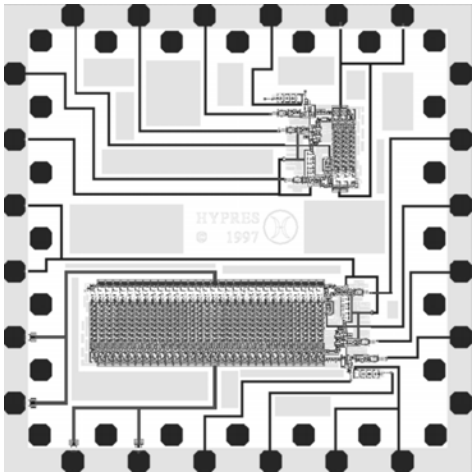


Fig. 4 Layout of a 30-bit TDC with a 8-word multi-hit FIFO buffer and output parallel-to-serial converter.

HYPRES is working on a multi-channel TDC with time resolution down to 12 ps and multi-hit resolution better than 24 ps. To enable the multi-hit capability, we have enhanced the simple binary counter-based design [10] with a first-in first-out (FIFO) buffer to store multiple time counts (Fig. 4). The small multi-hit resolution is achieved by interleaving the counter readout/reset operation with its counting operation. In order to detect the weak output pulses from the cooled event sensors, we have integrated the TDC with a high-sensitivity, sub-μA threshold noise SFQ pulse detector. A packaging effort is underway to demonstrate the first joint operation of the cooled visual light photon detector and the superconductive TDC.

The full-performance TDC has approximately the same aggregate data rate as the high-resolution ADC. HYPRES is working on a VME bus interface to perform all control and data acquisition functions necessary for TDC insertion into real physics experiment systems.

CONCLUSION

While approaching the specified performance goals for superconductor components of digital systems, HYPRES is shifting its attention to the development of enabling technologies: interfacing, packaging, and cryocooling. These are the least developed areas of superconductive electronics.

The on-going upgrade of HYPRES fabrication facilities [1] will allow us to fabricate LTS circuits with submicron lithography. This will improve flash ADC performance up to 8 effective bits at 10 GHz and 80 GHz clock, high-resolution ADC up to 22 effective bits at 10 MHz (Table I, last column), and TDC to better than 10 ps multi-hit resolution. The most important goal will be to increase integrated circuit complexity to open the way to new, even more exciting LTS digital applications.

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