# EXPERIMENTAL REALIZATION OF A RESISTIVE SINGLE FLUX QUANTUM LOGIC CIRCUIT

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## Abstract

An integrated circuit including all basic components of the recently suggested Resistive Single Flux Quantum (RSFQ) logic family has been designed, fabricated and tested successfully. The circuit includes a generator of periodic SFQ pulses, four buffer/amplifier stages for splitting, channeling and regeneration of the pulses, a detector/load stage, and universal RSFQ logic gate (here performing the NOT function). The 10 $\mu$m design rule circuit employs 13 active Nb - $Al_2O_3$ - Nb Josephson junctions with the critical current density $\sim 0.5$ kA/cm$^2$, externally shunted by Mo resistors with R 1 Ohm. The shunting provided critical damping of the junctions ($\beta_c \lesssim 1$) and reasonable ($\sim 500$ $\mu$V) $I_cR$ product. The circuit operation has been tested by measurement of dc voltages $\overline{V}_i$ across various Josephson junctions as functions of the dc current through the pulse generator. Correct and stable operation of the circuit for the clock frequencies from 0 to $\sim$30 GHz has been demonstrated.

## Introduction

Recently, much attention has been attracted to a new type of the Josephson junction digital circuits where the binary information is stored in form of the single flux quanta (SFQ), and transmitted in form of short voltage pulses with the area

$$\int V(t)\, dt \simeq \Phi_0. \qquad (1)$$

In contrast with earlier SFQ logic circuits (using, é. g., the Josephson transmission lines[1], the "flux shuttle" shift registers[2] or the parametric quantrons[3,4]) in the new circuits the SFQ pulses could be transferred along resistive rather than purely inductive lines, and later regenerated to their nominal amplitude (Eq 1) by the next circuit stages. The simplest amplification stage of this kind consists of just a single overdamped ($\beta_c < 1$) Josephson junction biased with a dc current I slightly below its critical value $I_c$ (some more complex circuits with the similar junctions[7-11] can be even more suitable for this purpose). Apparently the first device using this principle, the binary counter, has been suggested by Silver and coathors [5]. Later this device has been tested [6,7] to be operable at frequencies of the input pulses up to $\sim$100 GHz [6].

This success has motivated invention of more complex logic circuits; for example an AND gate based on the two - junction interferometer was suggested in Ref. 7. This gate, however, could hardly be practical because it requires time coincidence of the supershort (picosecond) SFQ pulses (Eq 1). In order to get rid of this problem, a new major step , a more precise defenition of representation of the digital imformation, was required.

This step was made by suggestion [9,10] to use two similar lines rather than one for the information transfer. The first line carries (quasi)periodic clock SFQ pulses, and the second, the signal pulses. The binary unity/zero is represented by presence/absence of the signal pulse within a time interval between two neighboring clock pulses. This representation allows one to design [9,10] a complete set of dc powered logic gates, including the NOR gate critical for virtually every Josephson junction logic family. Numerical simulation of these "Resistive Single Flux Quantum" (RSFQ) logic circuits has shown [9,10] that they can operate at clock frequencies up to 30 GHz using externally shunted tunnel junctions with quite available $I_cR$ products of order 300 $\mu$V.

The purpose of this paper is to report the results of the experimental test of all basic components of the RSFQ logic circuits, including a universal gate which can perform the NOR function sufficient in principle for design of an arbitrary complex logic circuit.

## Test Circuit: General Structure

Figure 1 shows the general structure of our test circuit. Periodic SFQ pulses from the clock generator G are regenerated and split by the buffer/amplifier $A_1$. Pulses from the port 1 of the amplifier serve to reset the NOT gate periodically. If no signal pulse arrives at the S input of the gate during a clock period, the gate produces an output pulse. Delayed by the stage $A_2$ and split by the stage $A_3$, this pulse arrives at the input S of the same gate. If the clock period T is not too short (is larger than the time delay $\tau$ of this loop circuit) this pulse will block production of the output pulse during the next clock period. Thus the properly operating circuit produces the gate output pulses each second clock period. The buffer stage $A_4$ unites this pulse train with the original pulse train from the stage $A_1$. Thus the average frequency of pulses arriving to the detector/load stage D equals $(3/2)T^{-1}$.

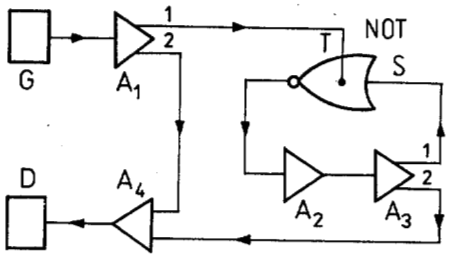


Fig. 1. Block structure of the experimental RSFQ test circuit: G, the SFQ pulse generator; $A_1$ - $A_4$, the buffer/amplification stages; NOT, the RSFQ inverter; D, the SFQ pulse detector/load stage.

## Test Circuit: Design and Simulation

Figure 2 shows the equivalent circuit of our device, and Figure 3, results of its numerical simulations using the COMPASS program [12] for experimental values of parameters and typical values of the dc bias currents $I_{in}$, $I_1$ + $I_7$.

The clock generator G consists of the junction $J_o$ biased by dc voltage $V_o$ arriving from small resistor $R_o$ through superconducting inductance $L_o$. The generated

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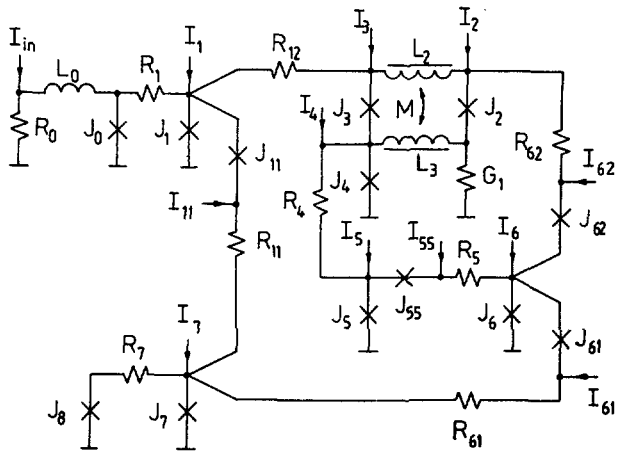



Fig. 2. The equivalent circuit of the test structure. Crosses denote overdamped Josephson junctions; arrows, dc bias current leads.

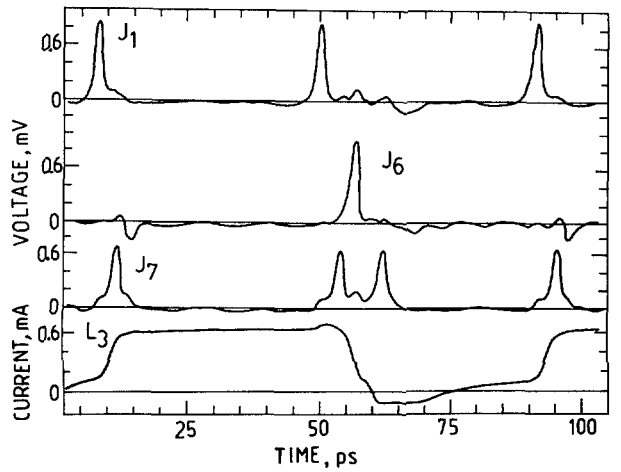



Fig. 3. Results of numerical simulation of the circuit shown in Fig. 2 for the experimental values of its parameters: ($I_{co}=I_{c1}=I_{c6}=I_{c7}=1$ mA, $I_{c4}=I_{c5}=0.75$ mA, $I_{c11}=I_{c2}$ $I_{c3}=I_{c55}=I_{c61}=I_{c62}=0.5$ mA, $I_1=I_{11}=I_3=I_{61}=I_{62}=I_5=0.4$ mA, $I_7=0.93$ mA, $I_{55}=I_4=I_2-I_4=0.2$ mA, $I_3-I_2=0.28$ mA, $R_1=R_{12}=R_{11}=R_5=0.2\Omega$, $R_o=0.3\Omega$, $R_7=0.5\Omega$, $R_{61}=1/G_1=R_4=0.25\Omega$, $R_{62}=0.1\Omega$, $L_o=8$ pH, $L_2=L_3=11$ pH, $M=0.6L_2$) and a typical value of the generator dc voltage $V_o=50$ $\mu$V resulting in the SFQ pulse frequency $f\simeq 25$ GHz.

SFQ pulses following with the time period $T=\Phi_o/V_o$ are passed to the buffer/amplifier $A_1$ comprising two junctions $J_1$ and $J_{11}$, dc biased below their critical currents. The arriving pulse induces $2\pi$-leap of the Josephson phase of the junction $J_1$, and is thus being reproduced with some gain. Junction $J_{11}$ provides unilateral properties of the stage, i.e., prevents injection to $J_1$ of pulses arriving from $J_7$ (see below).

The NOT gate [10] consists of a superconducting interferometer (including two Josephson junctions $J_2$, $J_3$ and the mutually coupled inductances $L_2$, $L_3$) connected with junction $J_4$ and resistor $G_1$. The interferometer has two alternative superconducting states differing by one flux quantum $\Phi_o$ in its loop, i.e., by the direction of the persistent current circulating around the loop. Dependent on the initial state of the interferometer, the arriving clock pulse induces the $2\pi$-leap of the phase of either junction $J_3$ or $J_4$. In the latter case, an output pulse is developed across the junction J4.

This pulse is delayed and regenerated by the buffer stage $A_2$ comprising junctions $J_5$ and $J_{55}$, and is split by the stage $A_3$ ($J_6$, $J_{61}$,$J_{62}$); dynamics of these stages is similar to that of the stage $A_1$. One copy of the pulse split by the stage $A_3$ follows to the S input of the NOT gate through the resistor $R_{62}$, while another copy arrives at the channeling amplifier $A_4$ through the resistor $R_{61}$. This amplifier $A_4$ consists of the active junction $J_7$ which regenerates the SFQ pulses arriving through both resistors $R_{61}$ and $R_{11}$, and of the circuit ($R_7$, $J_8$) which serves as a nonlinear passive load.

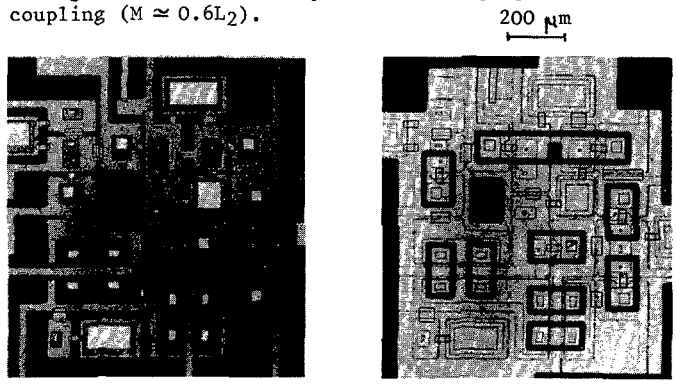
The SFQ pulses are very short and small (some 3 ps and 0.8 mV in our experiment), so that their direct observation presents a problem solvable only by rather complex techniques [13]. Thus we have used a method traditional for this field [6,7]: to determine average frequencies $f_i$ of the SFQ pulses in the given Josephson junction via measuring the dc voltage $V_i=\Phi_o f_i$ across it. According to the discussion of the previous section, in the properly operating test circuit the dc voltages across junctions should equal

$$\begin{cases} V_o, & \text{for } J_1,\ J_{61}; \\ (1/2)V_o, & \text{for } J_2 - J_6,\ J_{11}; \\ (3/2)V_o, & \text{for } J_7; \end{cases} \qquad (2)$$

within some range of the generator voltage $V_o$ starting from $V_o = 0$. In practice, we measured dc voltages across $J_1$, $J_4$, $J_5$, $J_6$, $J_{11}$, $J_{61}$, and $J_7$ as functions of the bias current $I_{in}$ of the generator.

## Test Circuit: Layout and Technology

Figure 4 shows photographs of a central part of the test circuit before and after formation of the counter electrode. The layout was carried out using 10 $\mu$m design rules and in particular employs 10×10, 10×15 and 10×20 $\mu m^2$ active Josephson junctions. The original design based on the figure $j_c = 0.1$ kA/cm$^2$ for the critical current density of the Josephson junctions used only two superconducting layers, and a series of auxiliary large - area Josephson junctions providing superconducting pathes between the layers. Relatively large inductances (including those of the interferometer) were formed as strips of one electrode crossing gaps in the other electrode; distance between the strips forming $L_2$ and $L_3$ was calculated to provide their proper inductive coupling ($M \simeq 0.6L_2$).




(a) (b)

Fig. 4. Central section of the test circuit (a) before and (b) after deposition of the counter electrode.

For fabrication of the circuit we used the Nb - $Al_2O_3$ - Nb Josephson junction technology described in detail elsewhere [14,15]. Figure 5 shows (schematically) a cross section of a fragment of our thin - film structure. The structure was deposited onto silicon wafer

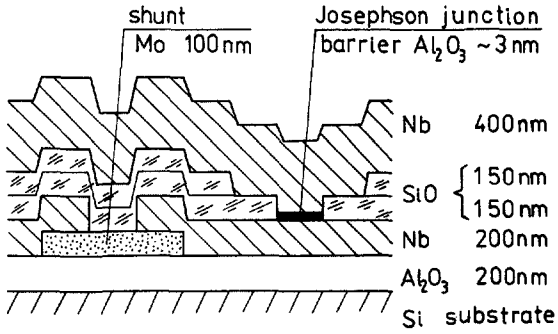



Fig. 5. Cross section of a representative part of the integrated circuit (schematically).

covered by a protective layer of $Al_2O_3$. The resistors were formed by chemical etching of Mo film with $(R_\square)_{4.2K} \approx 1\Omega$ ; liftoff was used to pattern the upper layers. The Nb films were deposited using magnetron sputtering, and the SiO insulation, using thermal evaporation. After opening windows in the latter layer, the surface of the base electrode was RF cleaned and covered by thermally evaporated Al thin film. The film was then thermally oxidized[15] and the counter electrode was deposited. The Josephson junctions fabricated in this way exibited satisfactory small parameter scattering ($\delta j_c/j_c < 5\%$ throughout a chip), low leakage conductances ($V_m > 10$ mV), and did not change their parameters after numerous thermal recyclings.

Unfortunatelly, the critical current density $j_c$ of the junctions at this first stage of experiments was close to 0.5 kA/cm$^2$, i.e., factor of five larger than planned during the test circuit design. This is why it was found appropriate to deposit an additional insulating 0.5 μm layer of the AZ 1350 photoresist and a Pb ground plane film over the whole structure. This measure reduced the inductances $L_2$ and $L_3$, and thus the $LI_c$ product of the interferometer to the value $2.5\Phi_o$ close to the planned one ($\sim 1.3\Phi_o$). This is why the maximum clock frequency of the circuit, according to our numerical simulations (Fig. 3), should be close to 50 GHz, a factor of $\sim 1.7$ less than could be achieved with same junctions for optimum values of the inductances.

## Experimental Results

The test circuit was activated at T = 4.2 K by consequent turning on of the dc bias of its stages, from the pulse generator to the detector. During this procedure the bias current of each stage was adjusted to provide its correct operation. In particular, turning out of the generator ($I_{in} \to 0$) should stop propagation of the SFQ pulses along all the circuit, i.e., result in zero voltage across all its Josephson junctions.

Figure 6 shows an example of such an adjustment for two neighboring stages a and b. If activated separately, the junctions of the stages exhibited I - V curves usual for overdamped junctions with close critical currents $I_c \simeq 1$ mA (the bottom plots). If the stage b was current biased somewhat below its $I_c$, the dc voltage across it could be induced by the current $I_a > I_c$, partly because of the SFQ pulse generation, partly because of resistive coupling of the stages. When the former mechanism prevailed, the dc voltages across the Josephson junctions of the stages where exactly equal. Qualitatively, a close behavior can be observed at the usual mutual phase locking of the Josephson junctions [16,17], but one should remember that in our case the "locking" is strictly one-directional: the SFQ pulses (i.e., the highly nonsinusoidal Josephson oscillations) of the junction a with $I_a > I_c$ induce the phase - locked pulses in the junction b with $I_b < I_c$, but not vice versa. When the both bias

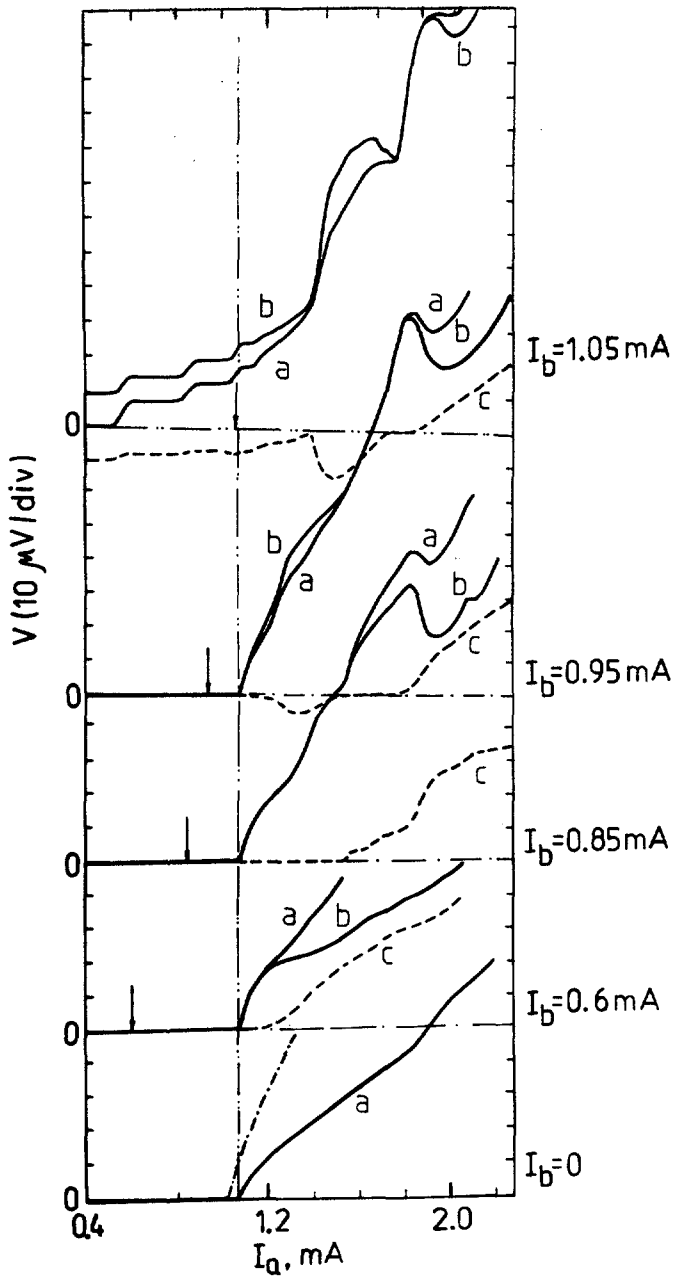



Fig. 6. DC voltages across Josephson junctions of two neighboring stages (G and $A_1$) of the circuit as function of one of the dc bias currents for several values of the second bias current. Dashed lines show the directly measured difference dc voltage $V_c = V_a - V_b$. Dash - dotted line shows $V_b$ as the function of $I_b$ for $I_a = 0$.

currents exceeded their critical values (see the top plots in Fig. 6), the phase locking could be observed as well, presumably of the mutual character here.

One can see that the SFQ reproduction in the stage b was especially stable at $I_b \simeq 0.85$ mA, so that this value was fixed. True, the activation of the following stages required some readjustment of the previously established values of $I_i$, but after some practice all dc currents could be properly fixed in few minutes.

In order to set up the bias currents $I_2$ and $I_3$, the critical value of $I_2$ was measured at first as a function of the difference current $I_3 - I_2$ changing the flux bias of the interferometer. The operation point was fixed just below a minimum of this (periodic) dependence, thus

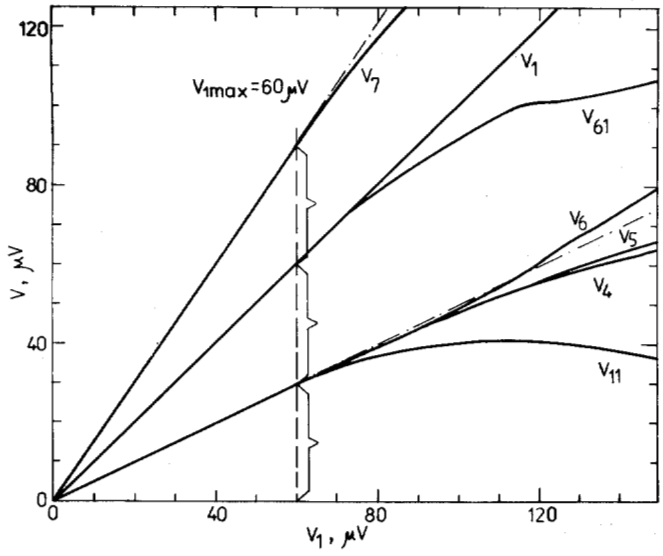



Fig. 7. Experimental plots of dc voltages $V_i$ across various junctions of the test circuit versus $V_1$ (see Fig. 2) obtained by slow sweeping of the generator current $I_{in}$. In the region $0 < V_1 \lesssim 60$ μV ($0 < f \lesssim 30$ GHz) where the relations (Eq 2) are fulfilled the test circuit is operating properly.

providing equal conditions for two stable states of the interferometer.

Figure 7 shows experimental plots of $V_i$ vs $V_1$ obtained by slow increase of the generator current $I_{in}$. One can see that the proper relations (Eq 2) between the dc voltages are fulfilled exactly (at least within the experimental accuracy better than 0.5%) until $V_1 \simeq 60$ μV, i.e., until the frequency of the generated SFQ pulses $f \simeq 30$ GHz. According to the both experimental and simulation results, at this frequency the channeling stage $A_4$ becomes too refractorary due to somewhat improper choice of its parameters.

## Conclusion

We have successfully demonstrated operation of a test circuit including all basic components of the RSFQ logic family at signal frequencies up to ~30 GHz. This encouraging result was obtained despite very simple layout of the circuit (two superconducting layers), large minimum feature size (10 μm), and a value of the critical current density far from the planned one.

Moreover, the further analysis have shown [11] that a considerable improvement of the RSFQ logic performance is possible owing to replacement of the coupling resistors by the Josephson junctions, and some modification of the logic gates. Accompanied by use of the modern junctions [17-19], these improvements can presumably allow one to create dc - powered high - density (~$10^{-6}$ $cm^2$/gate) digital integrated circuits with extremely high clock frequencies (up to 400 GHz), and moderate power consumption (of order $10^{-6}$ W/gate). We believe that these factors make the RSFQ logic family the most promising one in the whole Josephson junction digital technology.

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