NEW ELEMENTS OF THE RSFQ LOGIC FAMILY

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Abstract

Elements of the RSFQ logic/memory family have already reached operation frequency as large as 100 GHz and have a good chance to enter a sub-terahertz clock frequency range. Their parameter margins are as wide as ±25÷30%, even one bit gates possess flip-flop features, and can be naturally self-timed. In this report new RSFQ elements (OR-AND, NOR-AND, half adder, multiplexer, demultiplexer, and shift registers) are presented. Operation of these gates have been studied with the help of the Personal Superconductor Circuit ANalyzer (PSCAN) within the standard RSJ model of Josephson junctions. Parameter margins and other performance limits of the new elements are thoroughly investigated.

Introduction

It has been shown that the basic elements of the recently proposed Rapid Single Flux Quantum (RSFQ) logic family, based on overdamped Josephson junctions, can operate at extremely high clock frequencies - from 30-50 GHz for 10 μm Nb technology, and up to 500 GHz for sub 1 μm Nb technology. These results of numerical simulations[1-3] have already gained confirmation in experiments with single bit elements[4-6] and small integrated circuits[7] fabricated in 10-μm and 5-μm design rules technology.

With such rapid elements it is necessary to use specific design technique meant to increase device operational frequency up to that of elements and to make it independent of the device complexity. This problem was successfully solved by means of the asynchronous bit-level communications of basic gates[3]. It essence is a consistent transfer of well known pipeline and self-timing techniques to one-bit-processing level with using of the intrinsic memory inherent to each "logic" RSFQ element. This feature upgrades these elements to substantially reacher class of clocked flip-flops rather than mere logic gates. The elements of RSFQ logic, which were presented in two previous conferences[1,2], give possibility to build any logic devices but they do not cower a half of really existing ones.

The purpose of the present paper is to demonstrate technique to analyze RSFQ circuits, that enables us to introduce some new more complex RSFQ elements.

New elements

XOR cell

Essential features of RSFQ circuitry can be illustrated by the example of mentioned above[3] element (Fig. 1), which performs the two-input Exclusive Or (XOR) function. It includes storage interferometers J1, J3, L1, J5, J7 and J2, J4, L2, J5, J7, that are asymmetrically biased by current sources Ib1 and Ib2 respectively. As a consequence, each of them has two stable states ("0" and "1"), that differ by a single flux quantum, or, in other words, by directions of bias currents. Initially cell is in "00" state, i.e. both interferometers are in the "0" states with bias currents flowing through left arms of the interferometers; each of them can be triggered to the "1" state by single flux quantum Φ_0, or in other words, by single quantized voltage pulse V(t)

$$\int V(t)dt=\Phi_0 \qquad (1)$$

arriving from discrete Josephson transmission lines to its inputs A and B. Any of these events is accompanied by 2π-leap, at the junctions J1 or J2 and switch of the bias current to the common arm of the interferometers (Fig. 1c). Critical current of junction J5 in the right arm is larger than this flowing current, so the both states of the cell ("01" and "10"), induced by pulses A and B respectively, are stable. At the same time, this critical current is smaller than two switching currents, so arriving second pulse and switching second biased current to the right arm (state "11") induce 2π-leap of the junction J5, i.e. transition of this state to initial "00" one. So the current flowing through junctions J5 and J6 have only two different values which can represent logic XOR function of already present input pulses A and B. Due to large critical current output junction J7 does not switch at this time.

Now from third Josephson transmission line arrives pulse (1) at the input T. This voltage pulse induce current through pair of junctions J6 and J7, which cause 2π-leap either at junction J6 when cell is in "00" state, or at junction J7 in another states. Switching of the junction J7 not only generate quantum pulse (1) to the output line F, but also reset the cell in its initial state "00". Thus pulse T performs destructive readout the state of the cell.

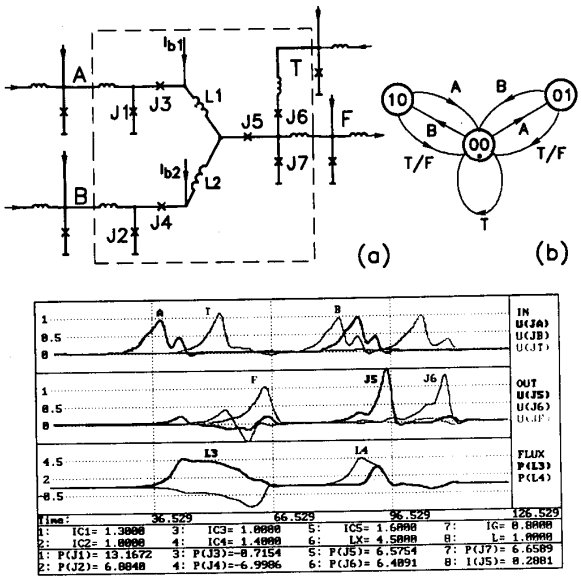

Fig. 1. Exclusive OR cell. (a) equivalent circuit (in dashed box) and schemes of its connection to discrete Josephson transmission line, (b) its state transition or Moore diagram (point marks initial state), and (c) screen view under numerical simulation of the circuit dynamics within the RSJ model (β_c =1) of the junctions using the PSCAN program (Ic1 designates critical currents for J1 and J2, Ic2 - for J3 and J4, Ic3.- for J5, Ic4 - for J6, and Ic5 - for J7; All critical currents are normalized by 100 μA, LX - dimensionless value of inductances L1 and L2 normalized by unit critical current, time unit ~1 ps for 5μm technology).

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One can see, that the cell can be considered as logic element only if accept the following basic RSFQ convention: *Arrival of the SFQ pulse to input terminal at the time interval between two neighbor SFQ clock pulses has a meaning of the binary "1", while absence of the pulse during this period is understood as the binary "0".* Note, that the convention does not require an exact time coincidence of the SFQ pulses. Moreover, a certain time sequence of the various input signals is not needed.

Physically dynamic of RSFQ circuit can be considered either as travelling, either trapping, or leaving single flux quanta through a underbiased overdamped Josephson junctions in more or less complex superconductor network. It is easy to qualitatively explain the choice of inductances, critical and bias current and other parameters of such network with desired features, but rather difficult to catch a convenient set of parameters without some specific tools. For these purpose these is specially designed Personal Superconductor Circuit ANalyzer (PSCAN) program, which allow one as first step of an analysis to observe dynamic on the screen (see Fig. 1b) and, if necessary, adjust parameters without interrupting the simulation. As next step, after some peculiarities of a circuit is found one can perform further optimization (see Appendix).

(A+B) • (C+D) Cell

As an exception, the AND cell does not require its own quantizing interferometer but can use those of the input cells, so that it is convenient to combine those to form one circuit performing a more general function

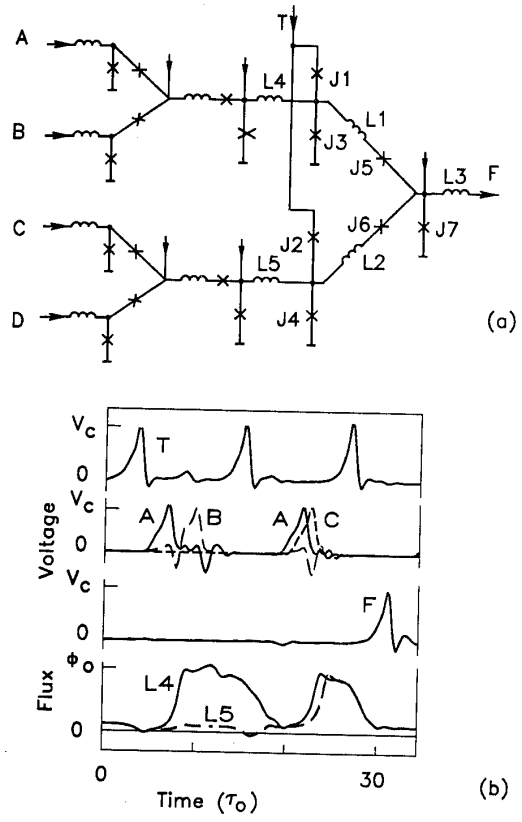

Fig. 2. Cell performing the generalized AND function F=(A+B) • (C+D): (a) equivalent circuit, (b) dynamics for two set of data: {A=B=1, C=D=0} and {A=C=1, B=D=0}.

Figure 2a shows an example of such a combined cell which performs the (A+B) • (C+D) function. Here the components J5, J6, L1, L2, J7 can be considered as forming the AND circuit, and the remainder as a couple of OR cells[1]. If both these OR cells are in their "0" state by the end of the clock period (which is possible only if A=B=C=D=0), the clock pulse T switches junctions J1 and J2, with no appreciable effect on the output F. If one of the OR cells (say, that with junction J3) is in its "1" state, then J3 (rather than J1) is switched by T, so that the SFQ pulse is applied to junctions J5 and J7 connected in series. The former of these junctions have a smaller critical current than the latter one, so that J5 is switched, and there is no output pulse again. The only case when J7 switches and produces the SFQ pulse in the output F is one when both OR cells are in their "1" state, so that both J3 and J4 are switched simultaneously by the clock pulse T. (In this case the pulse currents, injected to J7 through L1 and L2, sum up and exceed the critical current of this junction.)

Note that in contrast to all previous RSFQ cells, an exact time coincidence of the current pulses in L1 and L2 is essential in this circuit. However, this does not violate the RSFQ basic convention because these pulses are confined inside the cell; the input pulses A, B, C, D are free of this requirement. Numerical simulations show that the necessary coincidence is achieved inside a wide parameter window (the critical current margins can be larger than +30%). It is straightforward to modify this circuit by changing either one OR cell or both of them for cells performing other functions F1 and F2; in this case the combined cell will perform the function F1 • F2. In the specific case F1=OR and F2=NOR cells[1] the combined cell will be suit for ALU with functional structure as in Ref. 8. A "bare" AND cell is readily possible (with the DRO register cells in the both inputs); together with XOR cell it constitute the half adder.

Single Bit Multiplexer/demultiplexer

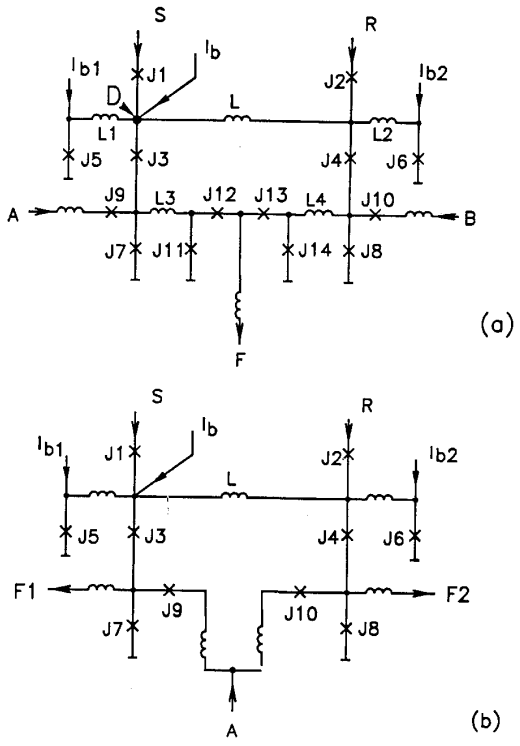

Fig. 3. Equivalent circuits of RSFQ (a) multiplexer and (b) demultiplexer. (Ic1=Ic2=Ic7=Ic8=Ic9=Ic10=Ic, Ic3=Ic4=0.4Ic, Ic5=Ic6=1.33Ic).

Since the RSFQ circuits communicate by SFQ pulses it is necessary to use special circuits for connection between them. Evident devices for transfer of the pulses are discrete Josephson transmission line and match microstrip line. For switching between such lines it is necessary to have multiplexers and demultiplexers. Of course they can be composed of the nondestructive read out register cells[2] (that can be transparent or not transparent for SFQ pulses in dependence on their intrinsic states) and split/confluence buffers discussed in Ref. 1. The special circuits, shown in Fig. 3, are, however, more convenient. Each of these very similar circuits is controlled by S/R pulses of the instruction code, which can switch state of the symmetric interferometer J7, J3, L, J4, J8 and thus establish what arm of it (right or left) becomes transparent for the signal SFQ pulses.

Each arm contains star of three Josephson junctions, (J3, J7, J9 in Fig 3a, as example). If current through the arm (junctions J3, J7) is small, the SFQ pulse from input A switches junction J9 without any pulse at the output F. In the opposite case the large current - will switch junction J7 instead of J9 and then due to small critical current - J3. Thus, phase at point D and therefore state of the cell does not change, but pulse come through confluence buffer J11 - J14 to output F. If in multiplexer the signal pulses A and B are independent, and are channeled to the common output F, then in demultiplexer (Fig. 3b) the common to both arm input pulse A is passed to one of the outputs F1, F2.

Cell Timing

Bit Level Elastic Pipeline

It is difficult to imagine that in the RSFQ (and any other) circuits with clock frequency more than 100 GHz would be possible to use global sichronization. We pointed out earlier[3] that extending well known elastic pipeline mechanism[9,10] to singe-bit-level of course could solve this problem. For this purpose each "logic" cell is accompanied by a coincidence junction, which asynchronously send output pulse and reset itself to initial "00" state just after second of the two input pulses has come [3]. Shift register with distractive read out register cells instead of logic cells is simplest structure of this kind (Fig. 4). Sections in the structure are connected by one data and two (SEND and ACK) clock lines.

Let the data occupy right sells of the register and all coincidence junctions are in a proper states due to SFQ pulses which have been sent to their inputs (Fig. 4). Now each SEND pulse fed into the right end of the structure read out data from edge cell and induces a shift of the data string by one step to the right, decreasing the data string length. On the contrary, an ACK' pulses fed into the left end (after data pulse if one put data signal 1) induces a rapid moving of the injected bit of data to the rightmost empty cell of the register, joining it to the data string that is not shifted during this operation. It is clear that this N bit elastic pipeline buffer allow one to have N clock period clock skew between its input and output that change only length of data string without any damages. Most intriguing are similar structure with logic elements, but shown one is also very useful for connection between superfast blocks.

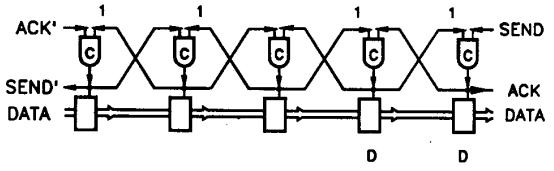

Fig. 4. Hand-shaking approach to the clock pulse distribution: the elastic pipeline mode of operation. D's denote cells with data. 1's - inputs of the coincidence junctions preset by SFQ pulses).

Simple Shift Register

Note that Fig. 4 show general approach that, in particular, is assumes that the data do not influence the clock pulse dynamics. In some specific circuits this rule can be somewhat violated, permitting very efficient designs. For example, Figure 5a shows a shift register which can be used in very compact cash memories (only two Josephson junctions per bit). The lower interferometers (J2, L4, J4, etc.) are quantizing and contain the data bits. The clock pulses T are propagating along non-quantizing loops of the upper row. If the pulse arrives to a junction column (say, J3, J4), that separates interferometers with similar states, it switches the upper junction (J3), because the persistent currents circulating in the interferometers cancel in the lower junction (J4) and it is far from its critical state. On the other hand, if the states differ (say, L4 does not carry the persistent current, this fact denoting binary "0", while L6, carries the clockwise current denoting "1"), the persistent currents sum up in the lower junction (J4), driving it close to its critical state. In this case the clock pulse switches the lower junction rather than the upper one. This event shifts the flux quantum (i.e., binary "1") from cell L6 to cell L4, and also somewhat influences the clock pulse dynamics, but does not change the very fact of the further propagation of the clock pulse (because switching of either J3 or J4 produces the SFQ pulse V(t) in the point D). One can check up that all "1"-"0" and "0"-"1" boundaries, and hence all the data string, will be shifted to the right after propagation of the single clock pulse along all the register.

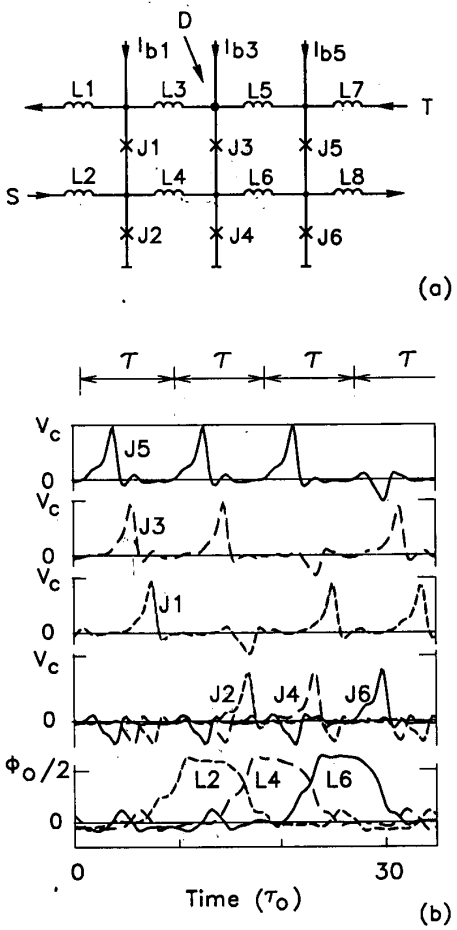

Fig. 5. A simple RSFQ shift register: (a) equivalent circuit and (b) dynamics for two cases described in the text.

Conclusion

The Josephson junction RSFQ circuits seems to represent the fastest digital technology available nowadays. Set of RSFQ cells (together with the cells introduced in this work) is well enough for building unique digital and analog/digital devices[11-12]. For instance, register cell shown on Fig. 5 very suited for vertical integration could help to overcome megabit level in Josephson memories. But in any case RSFQ sells with their intrinsic memories is almost ideal object for theoretical speculations about ultimate performance of digital electronics.

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Appendix. Approach to Parameters Optimization

For optimization one must prepare formal description of behavior of the circuit as scenario of switching of the Josephson junction under action of input and clock pulses. For XOR element (Fig. 1) this scenario can be listed as follow:

Begin of scenario. Circuit is in "00" state. At the input A arrive voltage pulse.
1. *Junction J2 switches.*
Circuit is in "10" state. At the input T arrive voltage pulse.
2. *Junction J7 switches.*
3. *Junction J4 switches.*
Circuit is in "00" state. At the inputs B and A arrive voltage pulses.
4. *Junction J2 switches, junction J1 switches.*
5. *Junction J5 switches.*
Circuit is in "00" state. At the input T arrive voltage pulse.
6. *Junction J6 switches.*
7. *Time is over.*
End of scenario.

PSCAN program could calculate the number of first incorrect act. The matrix of these numbers on the grid of two parameters solves problem of optimal value and margin of these parameters. However execution for each set of parameters take considerable time. For example, for the XOR cell (together with pulse sources and one stage Josephson transmission lines not shown in Fig. 1) this time equals approximately 20 second at a 20 MHz personal computer IBM PC/386. So this way is rather time consuming for two dimensional problem and practically unusable for multidimensional one. Much more practical and as we believe almost optimal iterative algorithm of parameter margin optimization is available:

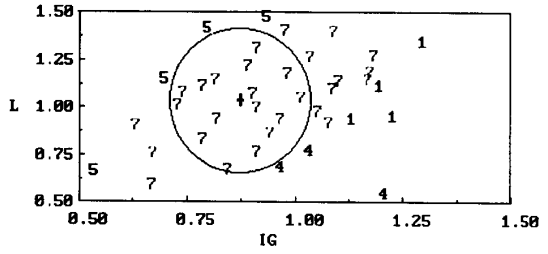

Fig. 6. Screen view while parameter optimization. Digit show scenario line failed first at the point, while 7 means successful operation.

Assume that result of simulation in N points has been obtained (see Fig. 6).
1. Now find the location of the largest elliptical area with definite ratio of axis (i.e. current largest operation range), which does not contain the "bad" points.
2. Find the point in this area which is most remote from other points. Run the procedure to probe this point.
3. If the result of simulation is OK then go to step 2, else go to step 1.

Moreover instead of carefully looking for positions of operation range and new point for verification, it is enough to generate several dozens of random points and choose accordance with the criteria the best of them. It is needed also to use more sophisticated rules of rating the position of the point at step 2, which take into account the ratio of distances to nearest good and bad points. This algorithm very quickly evaluate optimal value of parameters. So far the circuit with 20 Josephson junctions (Fig. 1) and for mentioned above computer consume less then half hour to optimize two parameters, several hours - tree parameters, and on round the clock - four parameters.

References

1. K. K. Likharev, O. A. Mukhanov, and V. K. Semenov, "Ultimate performance of RSFQ logic circuits", *IEEE Trans. on Magn.*, MAG-23, 759-762, March 1987.

2. O.A. Mukhanov, S.V. Rylov, V.K. Semenov, and S.V. Vyshenskii, "RSFQ logic arithmetic", *IEEE Trans. Magn.*, MAG-25, 857-860, March 1989.

3. O.A. Mukhanov et al., "Recent development of Rapid Single Flux Quantum (RSFQ) logic digital devices", Ext. Abstr. of ISEC'89, Tokyo, 1989, 557-560.

4. V.P. Koshelets et al., "Experimental realization of a resistive single flux quantum logic circuit", *IEEE Trans. on Magn.*, MAG-23, 759-762, March 1987.

5. V.K. Kaplunenko et al., "Experimental study of the RSFQ logic elements", *IEEE Trans. on Magn.*, MAG-25, 861-864, March 1989.

6. V.K. Kaplunenko et al., "Experimental study of the single flux quantum devices", in: Ext. Abstr. of ISEC'89, Tokyo, 1989, 411-414.

7. L.V. Fillipenko et al., "Experimental implementation of analog-to-digital converter based on the reversible ripple counter", Report PRP-10 at this conference.

8. S. Hasuo and T. Imamura, "Digital logic circuits", *Proc. IEEE*, 77, 1177-1193, August 1989.

9. C. Seitz, "System timing", in: C. Mead and L. Convey, "Introduction to VLSI systems", Reading, MA: Addison-Wesley, 1980, Chapter 7.

10. S. Komori, H. Takata, T. Tamura, F. Asai, T. Ohno, O. Tomisawa, T. Yamasaki, K. Shima, K. Asada, and H. Terada, "Elastic pipeline mechanism by self-timed circuits", *IEEE J. on Solid State Circuits*, SSC-23, 111-117, Feb. 1988.

11. S.V. Rylov, "Analysis of high-performance counter-type A/D converter using RSFQ logic/memory elements", Report PRP-1 at this conference.

12. K.K. Likharev and V.K. Semenov, "RSFQ logic/memory family: a new Josephson junction technology for sub-teraherts-clock-frequency Digital Systems", Submitted to *IEEE Trans. on Appl. Superconductivity.*