ULTIMATE PERFORMANCE OF THE RSFQ LOGIC CIRCUITS

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Abstract

A new family of dc-powered Josephson junction digital devices, the Rapid Single Flux Quantum (RSFQ) logic, is described. The devices use overdamped Josephson junctions and two-junction interferometers to store, pass and process the digital information presented in form of single flux quanta. We have carried out extensive numerical simulation of the dynamics of the RSFQ logic gates and of some more complex circuits including serial full adder and reversible shift register, within the standard microscopic-theory ("Werthamer") description of Josephson junctions. The minimum clock cycles of the basic RSFQ circuits turn out to be as small as 2.5 ps. The most promising ways to use the RSFQ logic circuits at the present stage of development of the Josephson junction digital technology are discussed.

Introduction

Throughout the development of the Josephson junction digital technology, two approaches using different representations of the binary information were competing. In most fabricated and tested circuits the binary unity/zero was coded by presence/absence of the dc voltage across unshunted Josephson tunnel junctions with hysteretic I - V curves. These "latching" circuits, however, need to be ac-powered and their reset to the initial (superconducting) state should be slow enough in order to avoid punchthrough effects. These factors limit the minimum clock cycle of the latching logic circuits to the level of several nanoseconds, despite their much shorter active switching periods [1].

On the other hand, the logic circuitry using presence/absence of single flux quanta (SFQ) in superconducting quantum interferometers to store the information are potentially much faster and more energy-saving. For example, the circuits based on the parametric quantrons [2-6] can apparently be used to reach the ultimate limit of the energy consumption in computation [7]. The devices suggested in Refs. 8, 9 lack this feature but in other aspects they are similar to the parametric quantrons. All these circuits are, however, not quite convenient in practice because they also require three-phase ac power supply and moreover they have a limited distance range of the information transfer during one clock period. The latter drawback can be avoided in ballistic devices proposed in Refs. 10, 11, but they are very complex, large in size and thus hardly practical.

Recently, several new "resistive" SFQ digital devices without ac supply have been proposed [12, 13] and tested experimentally [14, 15]. The basic feature of these devices is the transfer of information in the form of short voltage pulses V(t) with the area

$$\int V(t)\,dt \leq \Phi_o \qquad (1)$$

An overdamped Josephson junction biased by a dc current $I_b < I_c$, subjected to the pulse (1), performs a 2π-leap of its Josephson phase difference and hence reproduces (regenerates) the pulse. This reproduction feature enables one to pass the SFQ-coded information at any distance required and even to use resistive coupling of the adjacent logic gates [16].

This type of circuitry has been shown [16] to enable one to perform arbitrary complex processing of information, if one uses two rather than one lines for its transfer. One line passes the internally-generated (quasi)-periodic clock pulses (1), while the second line carries the similar information pulses. Such system permits a natural representation of the binary zero as the absence of an information pulse in the time period between two clock pulses, and simplifies drastically the design of the most critical invertor-type gates. Just recently the basic circuit elements of this "RSFQ" system have been successfully tested at clock frequencies up to 30 GHz [17].

The purpose of present work is to revise critically the basic circuits of the RSFQ logic in order to make them more rapid and enlarge their parameter margins. In the process of this optimization we have found it beneficial to couple the gates with Josephson junctions rather than resistors, so that the first letter of our earlier acronym RSFQ [16] may be now deciphered more adequately as "rapid" rather than "resistive".

In order to investigate workability of our new devices we have used the program COMPASS developed in our laboratory earlier for numerical simulation of Josephson junction circuits [18]. In order to study the ultimate speed performance of the circuitry, the Josephson junctions have been supposed to be high-j_c unshunted tunnel junctions with neglibly small capacitance parameter β_c [19] and have been modelled using the equations of the microscopic theory [20].

Basic RSFQ Circuits

Transmission / Amplification Line

Figure 1 shows the simplest circuit capable to transfer the SFQ pulses between the logic gates, with a considerable current (and hence power) gain if needed. All the overdamped junctions of the line are dc current biased somewhat below their critical currents I_c, so that an input pulse induces a running wave of 2π-leaps of the Josephson phases φ across the junctions. In order to achive a current gain, the critical currents of the junctions should increase (e. g., exponentially) along the line.

The dynamics and performace of such lines had been repeatedly studied earlier - see, e. g., Refs. 10, 11, 13. According to the results of these studies, the time delay τ of the SFQ pulse per stage of the line can be shorter than the natural time constant $\tau_o = \hbar/2eI_CR_N$ of the overdamped Josephson junction. For an unshunted tunnel junction operating at a temperature $T < 0.5T_C$, τ_o is directly related to the "gap voltage" $V_g = (\Delta_1+\Delta_2)/\hbar$ of the junction:

$$\tau_o = \hbar/(2eV_g). \qquad (2)$$

For a typical value $V_g = 2.8$ mV this time constant is close to 0.12 ps.

Time delay of the other basic RSFQ circuits are somewhat longer, so that there is not much sense in a careful minimization of τ.

Buffer Stage

Figure 2a shows the simplest nonreciprocal circuit allowing one to pass SFQ pulses in one direction (left to right) only. When the pulse arrives from the left, it induces the 2π-leap ("switching") of the lower junction J_2, while the upper junction J_1 remains in its initial state (Fig. 2b). If, however, the pulse arrives from the right, it increases the currents in the both junctions, and the J_1 with the smaller critical current is switched. Negative feedback provided by conductances of the pulse sourse and load circuits prevent simultaneous switching of the lower junction J_2, so that the voltage

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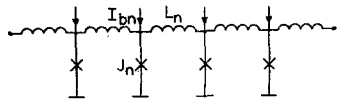

Fig. 1. Several stages of the transmission / amplification line for single flux quanta. $I_{bn} \simeq 0.7 I_{cn}$, $I_{cn}L_{n-1} \simeq 5\Phi_o/2\pi$.

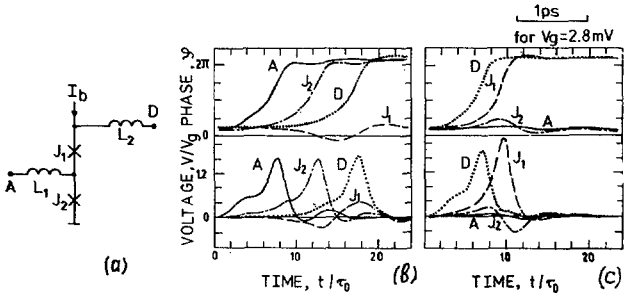

Fig. 2. Equivalent circuit of the buffer stage (a), and results of its simulation at arrival of the SFQ pulses from the left (b) and from the right (c) ports. The circuit values used in simulation are I_{c1} = 0.75 mA, I_{c2} = 1mA, $L_1 = L_2$ = 1.65 pH, I_b = 0.63 mA.

across it is virtually zero, i. e., the pulse does not pass to the left (Fig. 2c).

Figure 2b shows that the time delay τ introduced by the buffer stage is of the order of 2 time units τ_o defined by Eq. (2), which again is less than the delay of the more complex logic gates. Thus, the optimization of this circuit can be carried out starting from the parameter margin considerations rather than those concerning τ.

This stage is only one possible application of the pair of two overdamped junctions, of which only one junction is switched at a time by an arriving SFQ pulse. This "SFQ switch" is repeatedly used in all the RSFQ circuitry.

RS Flip-Flop

The main principle of the RSFQ logic suggests that the short SFQ pulse represents binary unity whenever it arrives during the longer clock period. In particular, the pulses arriving at inputs of a logic gate should not necessarily come simultaneously. This is essentially the feature which simplifies the logic family of RSFQ circuits drastically and makes them quite practical[16]. The only price for this advantage is that each logic gate of the family should remember the pulses arrived during the current clock period.

Figure 3a shows the simplest circuit of this kind which can be used as a RS flip-flop. It can be seen as a unification of two SFQ switches (Fig. 2a) and a two-junction interferometer using the lower junctions of the switches. The inductance parameter $2\pi I_c L_1/\Phi_o$ of the interferometer is close to 10, so at the given bias current $I_b \simeq 0.6 I_c$ the interferometer has two stable stationary states which differ by one flux quantum Φ_o trapped inside the loop and hence by the direction of the persistent current $I_p = \pm\Phi_o/2L_1$ circulating around the loop. The current I_b also provides the magnetic bias $\Phi_e = I_b L_1/2 \simeq \Phi_o/2$ and thus the equivalence of the two states.

In the initial stage the state of the interferometer corresponds to an anti-clockwise current I_p, so that the net current flowing through the junction J_1 is close to its critical value. The incoming pulse S switches this junction and thus changes the state of the interferometer to the opposite one, but does not penetrate to the output terminal O because of the large impedance of the inductance L_1 (Fig. 3b). Now the current through the junction J_2 is close to the critical value, so that if the pulse R arrives, it switches the circuit back to its initial state, simultaneously inducing a standard SFQ pulse (1) at its output O. Note that if two pulses arrive consequently from one input (S or R), the second of them switches the corresponding upper junction (J_4 or J_3) rather than the lower one, and hence does not change the state of the interferometer.

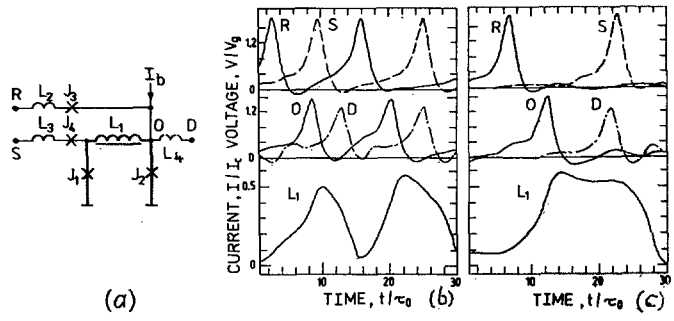

Fig. 3. Equivalent circuit of the RS flip-flop (a), and results of its simulations at period of input pulses $16\tau_o$ (b) and $32\tau_o$ (c). The circuit values used in simulation are $I_{c1} = I_{c2} = I_c$ = 1 mA, $I_{c3} = I_{c4}$ = 0.75 mA, L_1 = 3.3 pH, $L_2 = L_3$ = 1.65 pH, L_4 = 4 pH, I_b = 0.63 mA.

Figures 3b,c show the result of a numerical simulation of the dynamics of the flip-flop. One can see that the circuit retains workability for time periods as short as $\sim 12\tau_o$ (see Eq. 2). For the mentioned value of V_g (2.8mV) the minimum period is close to 1.5 ps, so that if the clock pulses T are used for the reset, clock frequencies as large as 660 GHz are possible (this result confirms the ealier estimate [16]).

RSFQ Logic Gates

OR Gate

Combining the SFQ switches and flip-flops, it is straitforward to design simple and fast logic gates performing all basic logic functions in the RSFQ representation. For example, the OR gate (Fig. 4) is merely a unification of one flip-flop and two additional buffer stages. The buffers feed one port (S) of the flip-flop with the SFQ pulses arriving from the two inputs A and B, and prevent the input circuits from undesirable mutu-

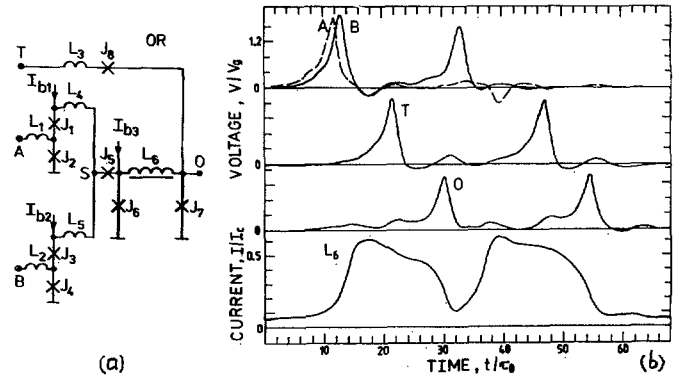

Fig. 4. Equivalent circuit of the OR gate (a), and results of its simulation (b). The circuit values used in simulation are $I_{c1} = I_{c3} = I_{c5} = I_{c8}$ = 0.75 mA, $I_{c2} = I_{c4} = I_{c6} = I_{c7} = I_c$ = 1 mA, $L_1 = L_2 = L_3$ = 1.65 pH, $L_4 = L_5$ = 1pH, L_6 = 3.3 pH, $I_{b1} = I_{b2} = I_{b3}$ = 0.63 mA.

al interactions. Figure 4b shows that pulses A in fact do not reach the input port B (and vice versa), and that the whole circuit is really functioning as an OR gate, producing the output pulse O just after the clock pulse T resets the flip-flop, if at least one of

the pulses A, B has arrived during the current clock period. Simulations show that the OR gate can operate with clock period as small as $\sim 12\tau_o$ (i.e., 1.5 ps for the above-mentioned value of V_g).

Invertor

Invertors (NOT gates) are the most critical logic circuits in nearly every Josephson logic family. It is especially true for the SFQ representation of information, where the invertor should produce the output pulse if the input pulse does not arrive. This is why the only circuit proposed ealier for this purpose (Fig. 11 of the Ref. 13) is so complex, slow and thus hardly practical.

Figure 5a shows a much simpler invertor circuit consisting mainly of the SFQ flip-flop, but with two series junctions rather than one in its right branch, of which the upper junction (J_4) has a smaller critical current. Thus if the input pulse S arrives, it switches this junction, and thus steers the persistent current to flow clockwise without induction of a noticeable pulse at the output port O (Fig. 5b). Now, when the clock pulse T arrives, it switches the junction J_2 rather than J_5 and hence does not pass to the output port. The same pulse after a small time delay by the circuit L_3, R, L_2 arrives at the port B and resets the flip-flop, also without induction of an output pulse. On the contrary, if the pulse S does not arrive during the current clock period, the clock pulse T finds the persistent current flowing anti-clockwise and the junction J_5 in a subcritical condition. Thus, this junction (rather than J_2) is switched, and an output voltage pulse O is formed across it (Fig. 5b).

It is straightforward to supplement the invertor with two or more input buffer stages (cf. Fig 4a) and thus to turn it to the NOR gate. Our calculations show that the clockperiod of the NOT/NOR gate can be at least as short as $\sim 18\tau_o$, i.e. 2.2 ps for V_g = 2.8 mV. This value is the largest one of those for all our basic logic gates, and this means that the upper clock frequency of the RSFQ circuitry is close to 450 GHz if only the basic functions are performed during one period.

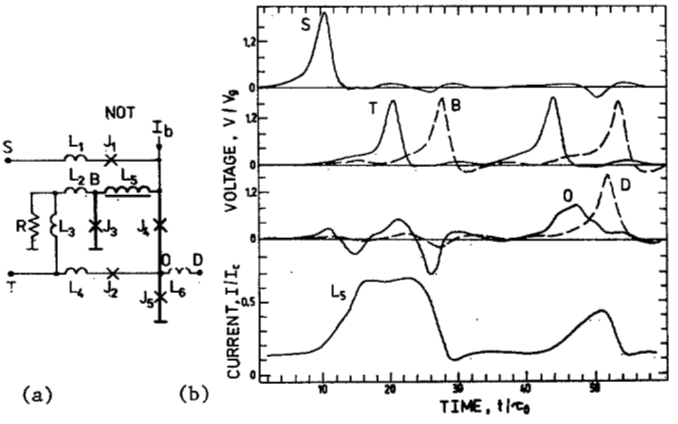

Fig. 5. Equivalent circuit of the NOT gate (a), and results of its simulation (b). The circuit values used in simulation are $I_{c1} = I_{c4} = I_{c5} = 0.75$ mA, $I_{c3} = I_c = 1$ mA, $I_{c2} = 0.8$ mA, $L_1 = L_3 = L_4 = 0.8$ pH, $L_2 = L_6 = 1.65$ pH, $L_5 = 3.3$ pH, $I_b = 0.63$ mA, R = 0.9 Ohm.

More Complex RSFQ Circuits

The effective speed of computation in the RSFQ devices can be, however, increased even further by using special ("functional") circuits for some more complex logic functions rather then composing the circuits in the regular way from the basic ones.

1 - Bit Full Adder With Carry Bit Store

Figure 6 shows an example of a very efficient functional RSFQ circuit. Its left part (L_5, J_5, J_6, and J_7) represents the SFQ flip-flop similar to those discussed earlier (cf. Fig. 3 - 5) but with each input pulse injected simultaneously into both branches of its interferometer. Due to this injection, each pulse changes the initial state of the interferometer to the opposite one. Thus this part of the circuit operates as a binary SFQ counter ("T flip-flop") quite similar in function to that discussed earlier [12], but with somewhat larger operation speed and wider margins. One can readily get convinced that if the pulses A, B and C represent two bits to be added and a carry bit, respectively, the correct sum bit pulse is formed across the junction J_7 under the action of the clock pulse T.

Moreover, the correct carry bit pulse is formed in the point G just after the second input pulse arrives. Unfortunatelly, this pulse cannot be used directly as the carry bit output, because the sum bit also penetrates there. The remaining part of the adder, including another flip-flop (L_9, J_8, J_{11}, J_{12}) serves to store carry bit and to cut off this parasitic signal. The genuine carry bit pulse steers the flip-flop current to flow clockwise, and thus is correctly read out to the port D_c under the action of the clock pulse T (which also resets the flip-flop). If the sum bit pulse is formed across the junction J_7 and switches the second flip-flop again through the superconducting path J_6, L_6, it also arrives to the buffer/delay circuit J_9, J_{10}, L_{10} and resets the interferometer again. This reset is achieved by switching J_{11} rather than J_{12} and thus does not yield an additional output pulse at the port D_c.

As a reward for these complications, the carry bit is formed after the end of the current clock period. Consequently it is possible to send this bit to the input S of the same circuit and thus to use it not only as an elementary cell of a parallel adder, but also as a very simple serial adder. Simulation showes that the minimum clock period of the adder is close to $36\tau_o$ (~4.4 ps).

Reversible Shift Register

Another very important functional circuit is the reversible shift register (Fig. 7). It consists of a chain of RS flip-flops (J_7, L_7, J_9 and J_{12}, L_{10}, J_{14}) storing bits in the form of single flux quanta and coupled by short transmission lines (L_8, J_{10}, L_9 and L_{11}, J_{15}). In order to obtain a shift by one cell from left to right, one should just feed the port RT with a single clock pulse, while a similar pulse fed into the port DT induces a similar shift in the opposite direction. Our calculations show that the maximum clock period of this device is close to $12\tau_o$ (i.e., ~1.5 ps).

Discussion

We have demonstrated that the RSFQ logic circuits can perform arbitrary logic functions with extremely short clock periods, about 2 ps per one basic (elementary) logic operation. This period is only a factor of three longer than that of the shortest process possible in the superconducting circuits, the 2π - leap of the phase difference across the overdamped tunnel junction. Thus it seems that these circuits are the most rapid ones possible in the Josephson junction digital technology.

Other important advantages of the RSFQ circuits include dc power supply, absence of large - size elements like transformers, and relatively large (~ 20%) parameter margins. Lastly, power consumption of a typical basic RSFQ gate (including dc bias source resistors) is quite

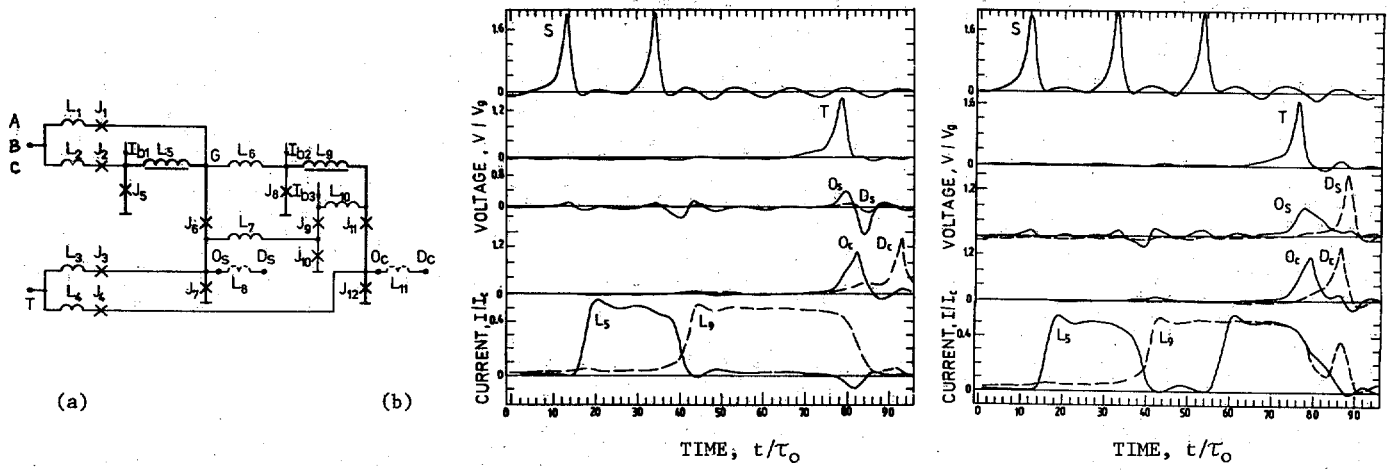

Fig. 6. Equivalent circuit of the 1 - bit full adder (a),and results of its simulation (b). The circuit values used in simulation are $I_{c1} = I_{c2} = 0.6$ mA, $I_{c3} = I_{c4} = I_{c5} = I_{c12} = I_c = 1$ mA, $I_{c6} = I_{c7} = 0.75$ mA, $I_{c8} = I_{c10} = 0.6$ mA, $I_{c9} = 0.4$ mA, $I_{c11} = 0.75$ mA, $L_1 = 1.3$ pH, $L_2 = L_8 = L_{10} = L_{11} = 1.65$ pH, $L_3 = L_4 = 0.7$ pH, $L_5 = L_9 = 3.3$pH, $L_6 = L_7 = 2.3$ pH, $I_{b1} = I_{b2} = 0.63$ mA, $I_{b3} = 0.3$ mA.

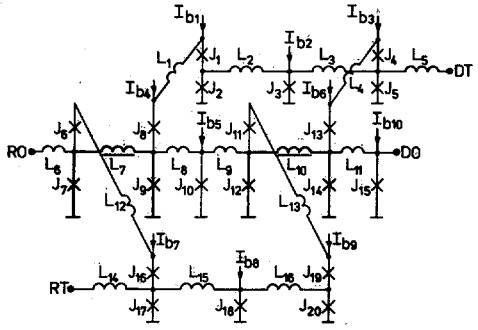

Fig. 7. Equivalent circuit of the reversible shift register.

moderate, of order one microwatt for reasonable parameter values.

All these features of the RSFQ logic circuitry give one a hope for the revival of Josephson digital devices. In the present - day situation in the field the best way to the revival seems to be design, fabrication and testing of a single - chip device with a performance high enough to justify its industrial production. Analysis shows that the most likely candidate for such a device could be an A/D convertor based on the SFQ "ripple counter" proposed by Silver et al.[12] (with further improvements[21]) supplemented by a RSFQ signal processor. In fact, the RSFQ circuits enable periodic read out of the current contents of the register of the converter at a high rate without stopping the counting, and to perform very fast real - time processing of the readings. One of the most valueable type of such processing could be a low - frequency filtering enabling one to improve the A/D conversion accuracy at relatively low - frequency signals [21].

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