TA 7.3: Superconductive Single-Flux Quantum Technology

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Key digital circuits for signal processing with tens of gigahertz speed and a few microwatts power dissipation have been recently demonstrated using a simple, 2μm linewidth process (Table 1). These are the fastest digital circuits reported to date [1, 2]. These circuits use novel rapid single flux quantum (RSFQ) technology that takes advantage of the fundamental properties of superconductivity [3, 4]. In this technology, data and clock are picosecond-long quantized voltage pulses corresponding to the transfer of single magnetic flux quanta, $\Phi_0 = h/2e = 2$ mVps. These SFQ pulses are regenerated at each gate and are processed by circuits comprised of overdamped Josephson junctions interconnected via microstrip inductances. The inherent internal memory of all RSFQ gates (primarily flip-flops), combined with high switching speed, makes serial, bit-pipelined circuit design advantageous. This paper presents experiments in RSFQ digital circuits, including an Nx8b serial multiplier*, and on-chip test systems based on RSFQ shift registers and on SFQ samplers. They enable test and study of RSFQ circuits at full GHz speed while communicating with semiconductor electronics at low speed.

The circuits are implemented using a standard 10-level Nb/AlOx/Nb thin film process with minimum Josephson junction (JJ) of 3.5x3.5μm² and a minimum linewidth of 2μm. This fabrication process is substantially simpler than semiconductor processes with similar design rules. The JJs are externally shunted with resistors to obtain a non-hysteretic IV-curve at a critical current density of 1kA/cm².

The logic diagram of a Nx8b-pipelined serial multiplier is shown in Figure 1. It consists of eight identical modules each comprising three types of RSFQ elementary cells: a latch with non-destructive read-out (NR), a latch (DR), and a serial adder (SA). These cells are interconnected with active Josephson transmission lines (JTL) providing SFQ pulse amplification and imposing the necessary controlled propagation delays. Figure 2 shows the logic diagrams corresponding to the functions performed by each cell and the schematics. Each module employs 48 JJs and dissipates 13μW. The multiplier takes N+K (K = 8 in this case) clock cycles to form the N+Kb product of an Nb data word and a Kb coefficient. It operates by an initial serial (or parallel) loading of the Kb coefficient into the NR registers. This can be done during the last K periods of the previous multiplication cycle. Then, the data word is applied serially with the least significant bit (LSB) first. In contrast to the similar design for the semiconductor logic, the clock SFQ pulses are also applied serially since the duration of the SFQ pulses (about 8 ps) is less than the propagation and cell switching delays. The designed clock rate (14.5GHz) is defined by the $\tau_3+\tau_4$ (about 65 ps) propagation delay between adjacent modules and the switching time of a 1b SA (Figure 1).

To test RSFQ circuits at full speed, two types of on-chip diagnostic circuitry are used. The first circuit is based on acquisition shift registers successfully operating at 18 GHz [1] (Figure 3a). It consists of input and output shift registers and a dual-frequency (MHz/GHz) clock generator. To convert data from (to) picosecond SFQ pulses and to (from) conventional external signals, SFQ/DC and DC/SFQ converters are used [3, 4]. The clock generator triggered by the low-power external clock provides circuit timing at high-speed (GHz range) and synchronous data exchange with room-temperature electronics at lower MHz speed. Figure 4 shows the layout fragment of the Nx8b multiplier integrated with this test system. Figure 5 shows multiplier operation at 6.3GHz with the 33MHz I/O data exchange with conventional electronics. High-speed test of the multiplier at maximum speed is in progress.

The second on-chip diagnostic circuit is an SFQ sampler (Figure 3b). The core of the variable-delay signal generator consists of the variable delay lines that are the simple 80-JJ JTLs (Figure 2b). These delay lines provide all input and clock SFQ pulses for the RSFQ circuit under test with picosecond delays set by their dc biases. Each RSFQ cell works as a coincidence detector. Applying a slow sweep current to the bias of one of the variable delay lines, the dc voltages across outputs is monitored, averaging the samples. The technique enables measurement of circuit response time, maximum clock frequency, and minimum required delay between input and clock pulses rather than the exact pulse waveforms. This technique is used to test the NR-cell of multiplier. A maximum clock frequency of 25GHz is attained.

All measured clock rates of the RSFQ devices are significantly higher than reported values for any semiconductor and for other superconductor technologies. Integration of these circuits with superconductive GHz-bandwidth A/D converter paves the way for a signal processor with performance parameters presently unattainable with any other technology [5].

Acknowledgments

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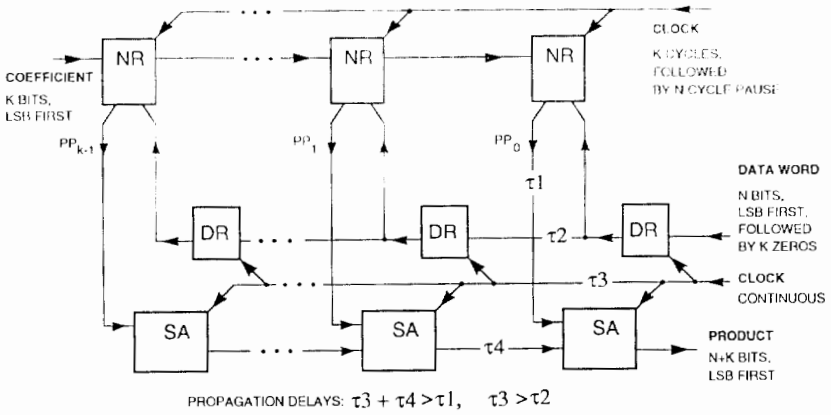

Figure 1: Bit-pipelined serial multiplier logic.

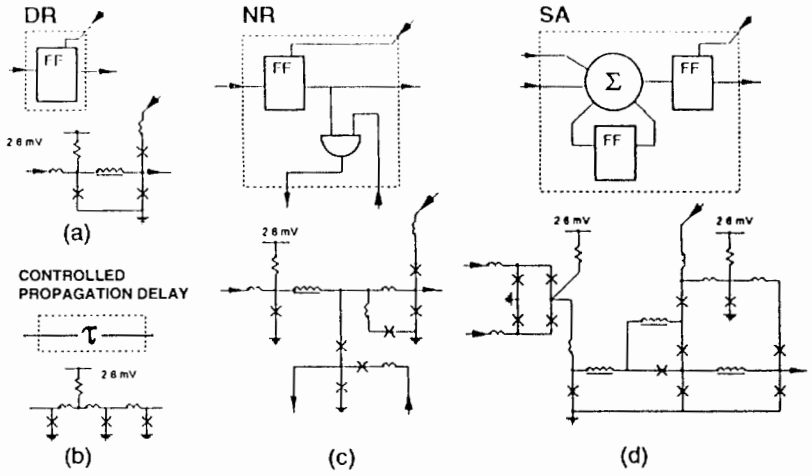

Figure 2: Detailed diagrams and schematics of serial multiplier blocks. Crosses designate the overdamped JJs. Underlined inductors designate memory loops.

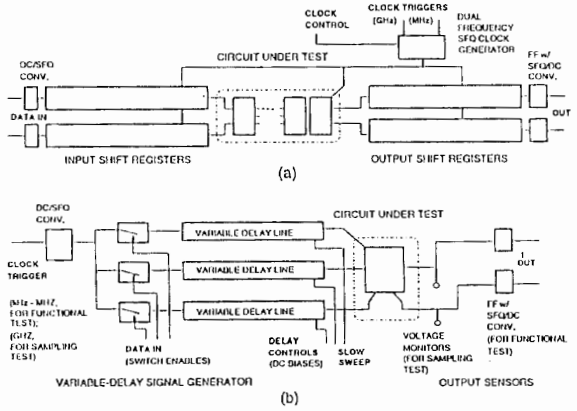

Figure 3: On-chip circuitry to test RSFQ circuits: (a) shift register based, (b) SFQ sampler.

Figures 4 and 5: See page 321.

Circuit	Size (bits)	Speed (GHz)	Power (mW)
Shift register:	4	60	0.004
	32	44	0.03
	512	20	0.5
	1024	19	1.0
Acquisition shift register:	32	18	0.04
	1024	16	1.0
Counter:	1	144	0.002
	12	120	0.016
1b half adder		23	0.006
2b full adder		13	0.013
Code correlator	128	16	2.0
8xNb serial multiplier		functional	0.1
		14.5	simulated

Table 1: RSFQ logic experimental results.