EXPERIMENTAL STUDY OF THE RSFQ LOGIC ELEMENTS

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Abstract

New elements of the Rapid Single Flux Quantum (RSFQ) logic family have been designed, fabricated and tested. All-Nb 14-layer 5 μm technology using externally shunted tunnel junctions with j_c = 500 A/cm², I_cR_s = 300 μV, and $\beta_c \leq 1$ has been employed. The T-flip-flop circuit has been demonstrated to operate with ±30% margins at clock frequencies below 50 GHz and with at least ±10% margins at the frequencies up to 120 GHz. Operation of the input (DC/SFQ) converter with ±40% margins and output (SFQ/DC) converter with ±40% margins is also demonstrated.

Introduction

The recently suggested[1,2] Rapid Single Flux Quantum (RSFQ) family of Josephson junction digital devices differs radically from the latching logic families by much higher operation speeds (clock frequencies). Already in the first experiments[3,4] which used 10 μm Nb technology, its basic components including NOR circuit, have been shown to operate properly at clock frequencies up to 30 GHz. The purpose of the present work was development and experimental study of two test circuits containing new members of the RSFQ family, including T-type flip-flop and two converters of digital information from the usual dc voltage form to the SFQ pulse form accepted in the RSFQ logic, and vice versa (some preliminary results of the study have been published elsewhere[4]).

Circuit Design

Test Circuit 1

Figure 1 shows microphotograph and equivalent circuit of the test circuit 1 designed for study of the SFQ T-flip-flop; it also includes generator of the SFQ pulse train, and the SFQ pulse transmission line.

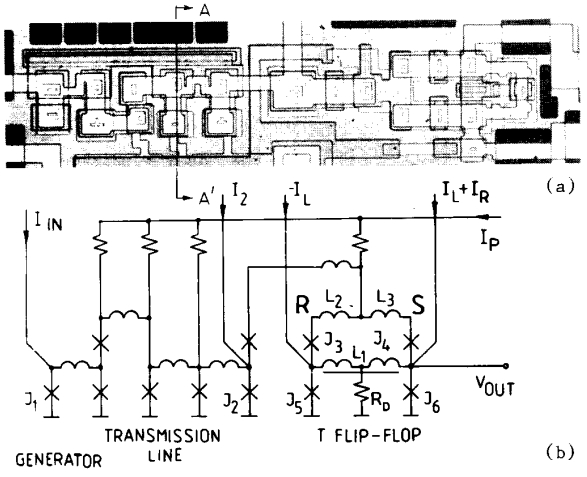

Figure 1. Test circuit 1: (a) microphotograph and (b) equivalent circuit.

Generator of the SFQ pulse train presents just an externally shunted (overdamped) Josephson junction J_1 biased by the dc current I_{in}. This current controls frequency f of the pulses which is directly related to the dc voltage V across the junction as $f = V/\Phi_o$.

Transmission line presents a consequence of the overdamped ($\beta_c \leq 1$) underbiased ($I \leq I_c$) Josephson junctions terminated by buffer stages[2]. Critical currents of the junctions and dc bias currents are increased gradually from left to right, so that the line not only transfers the SFQ pulses from the generator to the T-flip-flop but also increases their current amplitude (and hence energy $E \cong I_c\Phi_o$).

T-flip-flop differs essentially from the original version[5] of such a device by additional resistor R_d and a way of the input pulse injection. Numerical simulation shows that these measures can result not only in its larger operation speed but also in drastic increase of the parameter margins.

Test Circuit 2

Figure 2 shows the test circuit 2 designed for study of the DC/SFQ and SFQ/DC converters connected by a similar SFQ transmission line, and Figure 3 presents typical results of numerical simulation of the circuit operation.

DC/SFQ converter presents a two-junction interferometer with two stable superconducting states. If the input current I_{in} is increased to reach some value I_{on} (Fig. 3a), it switches the state of the interferometer (Fig.3b), so that an SFQ voltage pulse across junction J_8 is generated (Fig. 3c). In order to restore the initial state of the interferometer one can decrease

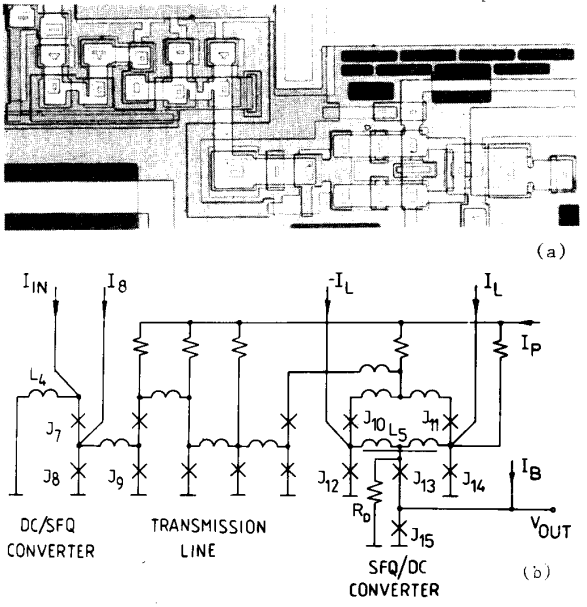

Figure 2. Test circuit 2: (a) microphotograph and (b) equivalent circuit.

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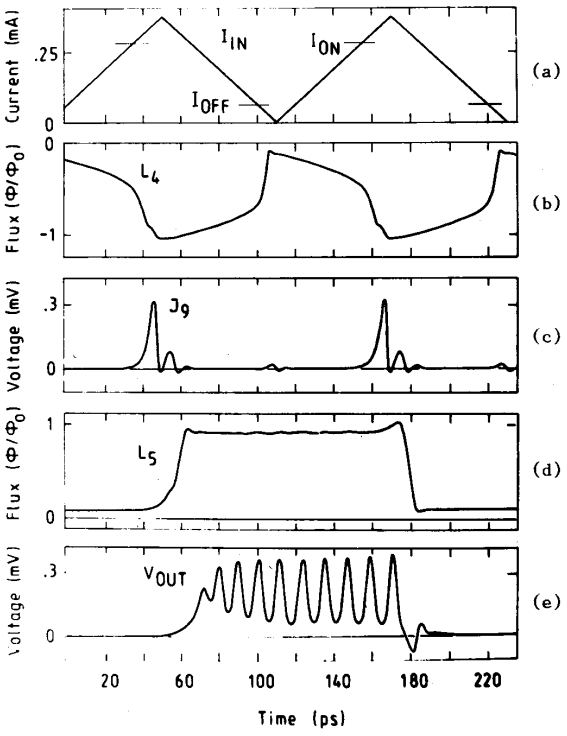

Figure 3. Results of numerical simulation of dynamics of test circuit 2 fed by triangle-wave current I_{in}, for the following set of parameters: $I_{c7} = I_{c8} = I_{c10} = I_{c11} = 0.75\ I_{c9} = 0.75\ I_{c12} = 0.75\ I_{c14} = 2\ I_{c13} = 2\ I_{c15} = 250\ \mu A$, $V_c = 300\ \mu V$, $R_d = 0{,}2$ Ohm, $L_4 = 0.5\ L_5 = 11$ pH.

I_{in} below another value I_{off}. Note, however, that during the restoration the SFQ pulse is generated across J_7 rather that J_8 so that it does not pass to the transmission line.

SFQ/DC converter presents the RSFQ T-flip-flop almost similar to the above described (Fig.1) but with an additional pair of Josephson junctions J_{13}, J_{15}., The change of the state of the base interferometer (J_{12},J_{14},L_5) of the flip-flop causes a π-change of the Josephson phase across the pair. Thus the critical current of the system as seen by the dc bias current I_b changes essentially. So one can readily choose a value of this current producing a nonvanishing output voltage V_{out} only at one state of the flip-flop. Action of this circuit is demonstrated by the results of its numerical simulation, which are shown in Fig. 3 d,e. Figure 3 shows that intrinsic delays of the DC/SFQ and SFQ/DC converters do not exceed 10 ps even when simple 5-μm Nb technology is employed.

Layout Design

We have fabricated our test circuits using several versions of all-refractory 5-μm design rule technology. Figure 4 shows a cross-section AA (Fig.1a). The layout differes in several aspects from the traditional one from our former Nb-AlO_x-Nb technology (see, e.g. Ref. 6).

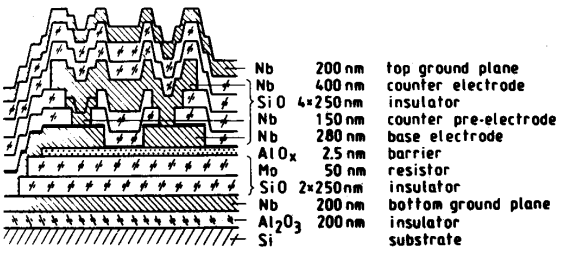

Figure 4. Cross-section of a typical part of our test circuits (e.g., across AA' line in Fig. 1a) - schematically.

Firstly, we have found that using two (top and bottom) ground planes we can noticeably reduce parasitic effects of external magnetic fields and currents on our circuits.

Secondly, it was found that external shunting of the junctions via additional SIN junctions used at the first stage of this work[4], has several disadvantages including necessarily large areas of the SIN junctions and complex dynamics of such shunting circuits. That is why a new operation allowing direct connection of superconducting electrodes to the resistor layer (Fig.4) was included in the technology.

Lastly, the layout included specially designed similar holes in the both ground planes for pinning the parasitic Abricosov vortices and filtering picosecond SFQ pulses.

Basic parameters of the circuits were measured using special test components.

Experimental Results

All measurements have been carried out at some temperature T within the range 4.2-6.0 K (the exact temperature was chosen to fix the critical current density at its nominal value). We have followed the same consequence of the circuit activation as described in Ref. 3 and 4.

Test Circuit 1

Figure 5 shows families of the "dc I-V curves" of the T-flip-flop for several values of the generator dc voltage V_{in} and dc flux bias $\Phi_b = I_L L_1$. The horisontal current step corresponds to equality $V_{out} = V_{in}/2$, i.e., to the correct operation of the flip-flop.

One can see that at "low" frequencies f of the SFQ pulse train ($V_{out} < 50$ V, i.e. $f < 50$ GHz) the circuit operates within very large parameter margins: $\Delta I_R/I_R = \pm 30\%$, $\Delta\Phi_b = \pm\Phi_o/4$. Moreover, there exists an additional operation range extending up to 150 GHz, separated from the basic one by a dead gap centered to 70 GHz. The gap has been proved to be caused by self-resonance of the basic interferometer of the flip-flop, which was underdamped due to drawbacks of the external shunting of the junctions via the SIN junctions (see above). In the final version of our technology (Fig. 4) this drawback was removed and the dead gap has disappeared and the operation range extended up to 120 GHz.

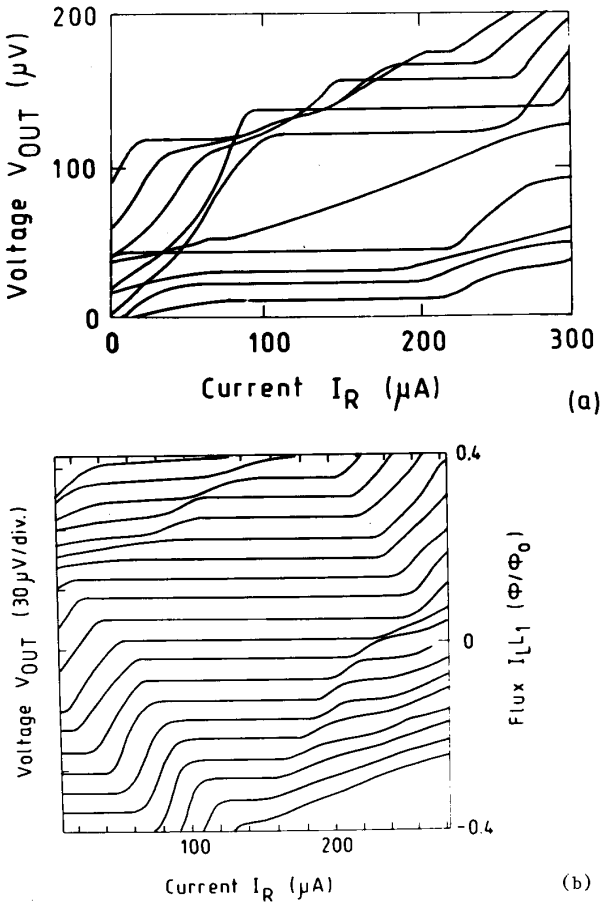

Figure 5. DC voltage V_{out} of the test circuit 1 as a function of the bias current I_R (Fig. 1b) for various values of: (a) input current I_{in} which determines the SFQ pulse train frequency f; (b) dc bias flux $\Phi_b = I_L \cdot L_1$ for fixed f ≅ 60 GHz. Note vertical shifts of the origin for the latter family of curves; left vertical scale shows values of corresponding to the horisontal current steps.

Test Circuit 2

Figure 6 shows the "dc I-V curves" of the SFQ/DC converter for two possible stable states of the basic T-flip-flop. One can see that the critical value of I_b is in fact effectively modulated $I_{c1} - I_{c0} \cong 0.4(I_{c1} + I_{c0})$.

Fixing I_b in the middle of this range one can test operation of both DC/SFQ and SFQ/DC converters by simple sweep of the input current I_{in}. Figure 7a shows a result of such an experiment (cf. Fig.3a,c,e). Despite vanishing dc voltage across the transmission line (the middle trace in Fig.7) the output dc voltage follows changes of the state of the T-flip-flop, which are induced by generation of the SFQ pulses at $I_{in} = I_{on}$.

If the amplitude of the sweep is increased, the second SFQ pulse can be generated at $I_{in}=I'_{on}$ ($I'_{on} = I_{on} + \Phi_o/L$, see Fig.2b). Such generation results in a

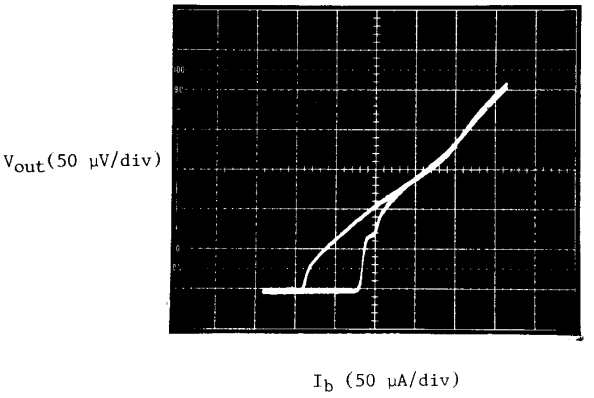

Figure 6. DC voltage V_{out} of the test circuit 2 as a function of the dc bias current I_b (Fig. 2b) for two possible states of the SFQ/DC converter.

behaviour shown in Fig. 7b which can be used to determine the operation margins of the DC/SFQ converter: $\Delta I_{in}/(I_{in})_{opt} = \pm 40$ %.

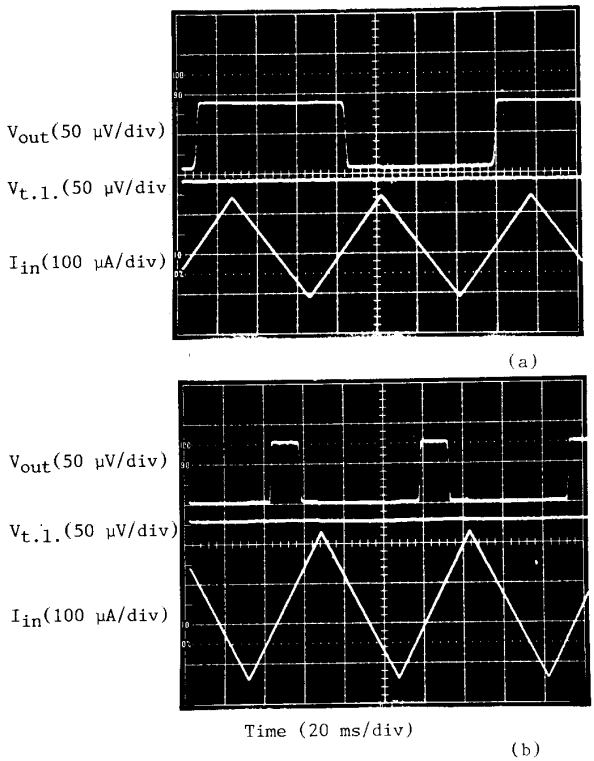

Figure 7. Time dependence of input current I_{in} of the test circuit 2 (lower traces), dc voltage across junctions of the transmission line (middle traces) and output voltage V_{out} (top traces) for two sets of parameters of the input current sweep. The measured values of threshold currents are I_{on}= 10 μA, I_{off}= -100 μA, I'_{on} = 150 μA.

Conclusion

We have demonstrated wide-margin operation of several new components of the RSFQ logic circuits including converters which can couple the circuits with the digital environment handling information in the usual dc voltage form. In practice speed of the conversion will be determined by this environment rather than the superfast RSFQ circuitry. The contrast of these speeds will determine a very specific general structure of the RSFQ integrated circuits[7].

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