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SFQ 6-ps Time Digitizing System

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Abstract—We have developed a high-performance 6-ps time digitizer system using a superconductor technology. The system employs a 2-channel RSFQ multi-hit Time-to-Digital Converter (TDC). The system is integrated with a semiconductor VXI interface and control modules. The TDC operation and output digital data analysis are performed and fully controlled using custom PC-based LabVIEW™ software. Each TDC channel has two parts: an All-Digital counter with a 3-hit, 14-bit buffer running at 20-GHz, and an 8-bin analog prescaler, which works as a vernier scale. We present preliminary designs, results of operation and experimental performance evaluation of this system.

I. Introduction

There are a number of applications that require very high time resolution – for example, time-of-flight (TOF) systems for nuclear and high-energy physics (HEP). Today, Rapid Single Flux Quantum (RSFQ) electronics can provide up to a 6-ps time resolution using present Niobium (Nb) trilayer technology [1]. Eventually, this Nb technology will surpass the 2-ps resolution level, given modest improvements in lithography. This extraordinary time resolution can be accomplished using less than 0.5 mW of power dissipation per TDC channel. Moreover, Nb technology is naturally radiation hard [2], enabling measurements in harsh accelerator laboratory environments. This report describes progress in design and testing of a 2-channel prototype TOF system (Fig. 1) being developed for Fermi National Accelerator Laboratory (FNAL). This system will be used for feasibility studies of Muon cooling.

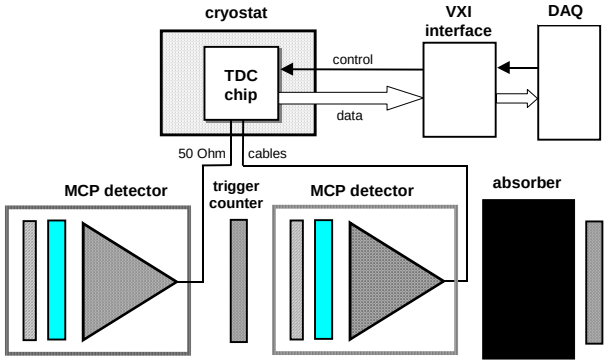

Fig. 1. Block diagram of the prototype TOF system. In this design, cosmic ray muons trigger micro-channel plate (MCP) detectors providing the start and stop events for the superconductive TDC chip.

II. Chip Design and Layout

This Time Digitizing System consists of two parts, a Coarse TDC that has been described in [3] and a Fine TDC, which has been described in [4]. Fig. 2 shows a block diagram of a single TDC channel.

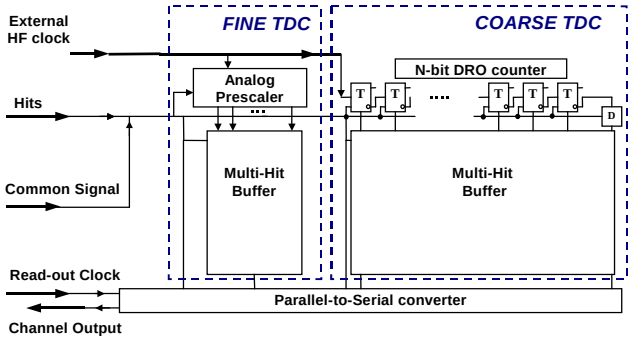

Fig. 2. A single channel of the multi-hit TDC, showing the coarse and fine components, as well as the I/O and control channels.

The design of the coarse TDC exploits the ability of RSFQ binary counters to operate at very high clock frequencies. [3] This speed allows us to perform time digitization by the direct counting of high-speed clock pulses. This feature makes the TDC's time resolution equal to one clock period. A two channel multi-hit TDC is shown in Fig. 3.

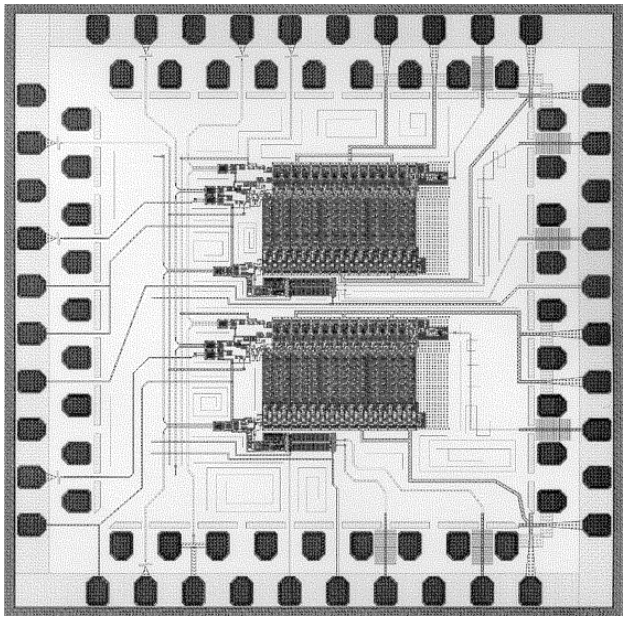

Fig. 3. Two-channel digital multi-hit TDC

The recorded hit data is read out from the TDC chip via a parallel-to-serial converter. The advanced circuit design used

allows the FIFO hit buffer to operate, even in case of a data overflow. The readout/interface electronics are controlled with a custom-built VXI-TDC control module. This interface generates all the control signals necessary to operate the TDC chip, including both data acquisition and readout channels. Data from the TDC chip is received and stored in VXI-based memory, then made available to the data acquisition controlling PC.

At 20 GHz, the digital counter or Coarse TDC provides a resolution of only 50 ps. Additional resolution is provided by an analog prescaler. [4] This prescaler races anti-parallel pulses along delay lines and uses a dynamic AND gate (Fig. 4) to determine the exact crossover point between one of eight equally spaced bins. The prescaler has been optimized for a 20 GHz clock and thus provides 6 ps resolution (50 ps / 8).

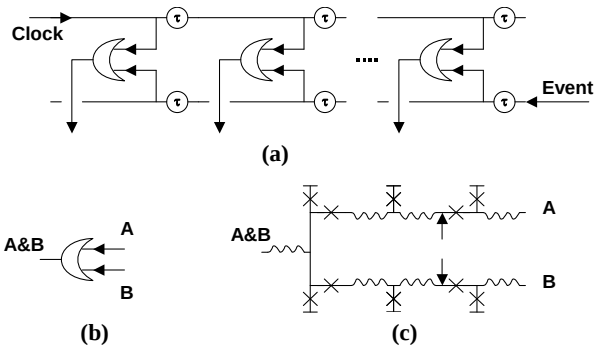

Fig. 4. (a) The dynamic AND prescaler uses anti-parallel pulse propagation. The time vernier is connected to dynamic AND gates. The symbol and schematic for this novel gate are shown respectively in (b) and (c).

We have experimentally observed reliable performance from the Coarse TDC chip at clock speeds up to 33 GHz [3], relying on the standard 3-μm 1 kA/cm^2 HYPRES fabrication process.

III. Exerimental results

This coarse TDC system and VXI interface was also tested with hits from an HP-8000 data generator. Hits were produced 4.3 ns and 28 ns apart, respectively, with a 20 GHz clock. The intended target was set for 4 ns and 26 ns, respectively; however, our TDC system unambiguously showed that the test pattern generator was out of calibration. This TDC measurement was verified using a Tektronix 3-GHz oscilloscope (Fig. 5).

IV. Conclusion

The completed version of the TDC system with two channels on a 5 mm x 5 mm chip is scheduled to be installed at FNAL later this year. Planned future improvements in the HYPRES fabrication process will make it possible to improve the time resolution of this system to 2 ps.

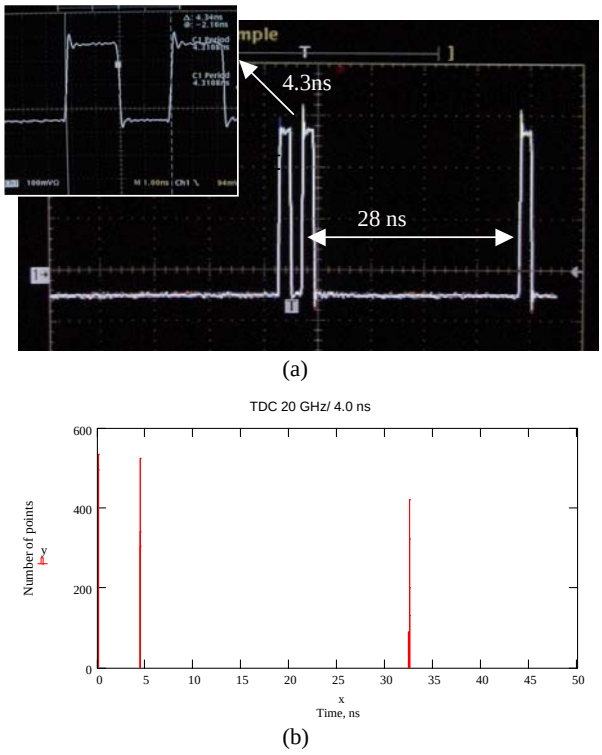

Fig. 5. (a) Hit pattern generated using HP-8000 observed on a Tektronix oscilloscope. (b) Histogram obtained from the measured data using the VXI data acquisition software shows the correct time between hits.

Acknowledgment

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References

[1] The standard HYPRES Nb process flow and design rules are available directly from HYPRES, or via the HYPRES web site at http://www.hypres.com/.

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