Superconductor Digital-RF Electronics

Oleg A. Mukhanov

***Abstract*— Unparalleled performance of superconductor digital and mixed-signal circuit technology enables the implementation of digital-RF architecture, which advances digital processing from baseband to RF stages. In this architecture, analog parts of RF systems are eliminated and replaced by digital circuits. The RF signal is directly converted to/from digital domain using superconductor oversampling analog-to-digital/digital-to-analog converters (ADCs/DACs). Digital signal processing (DSP) is performed on a single-bit oversampled digital RF data stream using high-speed RF DSPs rather than on multi-bit baseband data using conventional lower-speed DSPs. HYPRES is developing circuit components for digital-RF communication transceivers, including low-pass and band-pass ADCs, DACs, digital decimation and interpolation filters, digital correlators, digital up/down-converters, etc. All of these are based on ultra-fast Rapid Single Flux Quantum (RSFQ) digital technology. Highly linear (>100 dB) ADCs, ultrafast digital down-converters and digital filters operating at >20 GHz clock have already been demonstrated. A complete digital-RF receiver system has been integrated and cryopackaged on a commercial cryocooler.**

I. Introduction

Digital applications have always been the most coveted but yet the most difficult to realize into practical systems in superconductor electronics. Inherent advantages of superconductivity in speed and power were marred by impracticality of liquid Helium cooling and relatively low available integrated circuit (IC) complexity. Massive development of CMOS digital electronics has been continuously raising the level of competition and taking away possible market entry points from digital superconductivity. However with nearing the natural end of CMOS expansion governed by Moore's law, new opportunities started to appear in various areas of digital applications [1]. Even more prospects became apparent with emergence of new digital and mixed-signal applications requiring performance beyond physical limits of semiconductor technology.

Among these new applications are perspective military and commercial RF systems for communications, radar, and electronic warfare, which require wider bandwidth, better spectrum utilization and agility, use of more complex waveforms and higher frequencies. The realization of these new systems demands expanding digital technology into RF domain usually occupied by analog technology. Speed, power, linearity, sensitivity of superconductor RSFQ digital and mixed-signal circuits coupled with availability of robust IC fabrication process and commercial cryocoolers present an opportunity to introduce a relatively small-scale RF system based on a few RSFQ ICs and cryopackaged onto a compact cryocooler.

O. A. Mukhanov is with HYPRES, Inc., 175 Clearbrook. Rd., Elmsford, NY 10523 USA.

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II. Digital-RF Concept

Digital-RF architecture implies performing data conversion and digital processing at RF rather than at conventional baseband domain. Fig. 1 shows a block diagram of multi-channel, multi-mode, multi-band Digital-RF transceiver, in which RF signals are being converted to/from digital form directly at antennas. Such architecture can be realized only if both analog-to-digital and digital-to-analog converters (ADC and DAC) and digital processing circuits can deliver sufficient performance and can operate at a very high clock rate (20 GHz or higher).

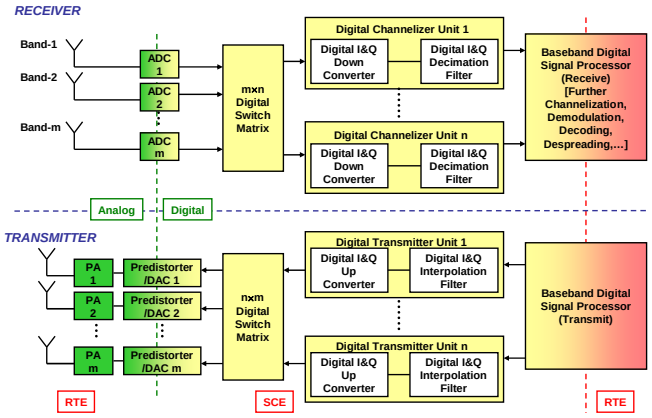

Fig. 1 Block diagram of Digital-RF Transceiver using combination of room-temperature electronics (RTE) and cryogenic superconductor electronics (SCE) elements located on different temperature stages of a cryocooler.

III. Recent Progress

A. Analog-to-Digital Converters

High performance ADC is the toughest challenge for Digital-RF systems. Substantial efforts are on-going to develop superconductor ADCs meeting requirements of Digital-RF systems [2]. Fig. 2 shows a performance plot, which compares semiconductor and low-pass superconductor, state-of-the-art ADCs.

One of the key advantages of superconductivity is the availability of high speed and very low jitter clock that can be integrated on the same chip as an ADC [3]. This would allow us to implement ADCs with higher performance (see dashed lines in Fig. 2) otherwise limited by the clock jitter.

High speed of RSFQ logic enables building oversampling band-pass ADC designs for direct conversion of RF signals with multi-gigahertz center frequencies, e.g. 5 GHz, 7.5 GHz. This is well beyond of limits of semiconductor ADCs.

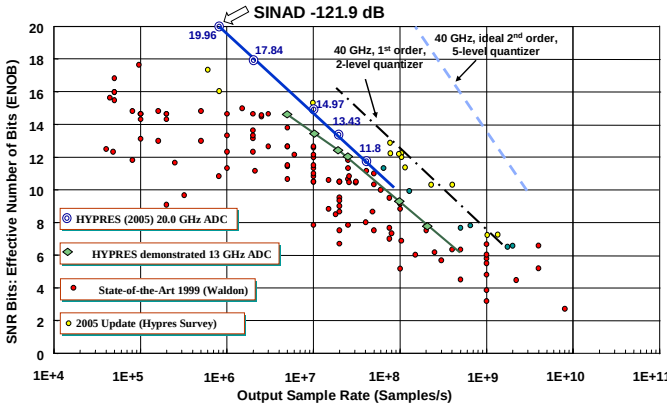

Fig. 2 Plot of signal-to-noise ratio (SNR) bits (or ENOB) versus sample rate (for signal at Nyquist frequency) for ADCs from Walden, recent ADC data, and HYPRES results. Solid lines – measured data for HYPRES low-pass delta ADC chip fabricated using 1.0 kA/cm^2 process. Dashed lines – projected performance for higher order multi-bit ADC fabricated using 4.5

B. Digital Receivers

The low-pass ADC modulator is used in an RF channelizing receiver based on Digital-RF architecture – All-Digital Receiver (ADR) chip (Fig. 3). A wideband RF signal is being applied directly to the ADC modulator producing oversampled one-bit data stream at tens of gigabits per second. This data is digitally mixed with a digital local oscillator signal to produce in-phase (I) and quadrature (Q) data streams [4] which are in turn applied to a couple of 15-bit decimation digital filters to reduce the sampling rate, narrow output bandwidth, and generate additional bits.

For the first version of the ADR chip, a 20 GS/s low-pass phase modulation-demodulation ADC modulator is used to deliver optimal performance for RF signals from dc to 175 MHz. This 12,000 Josephson junction chip was fabricated using 1.0 kA/cm^2 fabrication process and successfully tested up to 20 GHz clock. This design is being extended into a multi-chip module 2-channel version integrating a single ADC modulator chip and two channelizer chips. The 20 GS/s low-pass ADC modulator chip can be further replaced by a 40 GS/s version to achieve higher performance or by a band-pass ADC design to target higher RF frequencies.

The ADR chip (Fig. 3) is integrated into a hybrid-temperature, hybrid technology ADR test unit shown in Fig. 4. A special cryomodule is developed to package this ADR chip onto commercial 1.2 kW Sumitomo SRDK 101D cryocooler capable of cooling 125 mW at 4.2 K. The cryomodule solves complex issues of thermal management, magnetic shielding, and electrical noise. It is mounted into a standard 19-inch rack, which also houses cryocooler compressor, compact PCI chassis, computer monitor, and computer controlled dc bias current source. The cPCI chassis contains an interface amplifier module to amplify low-voltage output digital signals and to convert them to the TTL format, a channelizer module based on commercial PENTEK board to provide the 2nd stage channelization to smaller bandwidths, and a multi-channel board to provide acquisition of the ADR chip monitor data for setup and troubleshooting. Graphical user interface software is developed to perform setup, control, acquisition, and analysis of the received data.

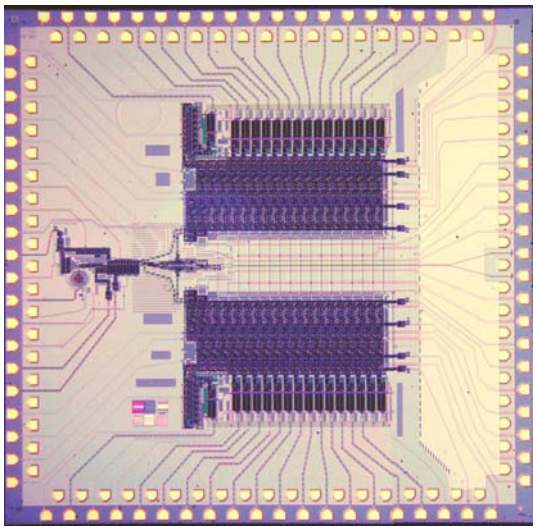

Fig. 3. Microphotograph of a single-channel All-Digital Receiver (ADR) chip based on the first-order low-pass delta ADC, digital in-phase and quadrature (I&Q) mixer, and decimation digital filters. This 1 x 1 cm^2 chip consists of ~12,000 JJs and dissipates ~3.5 mW.

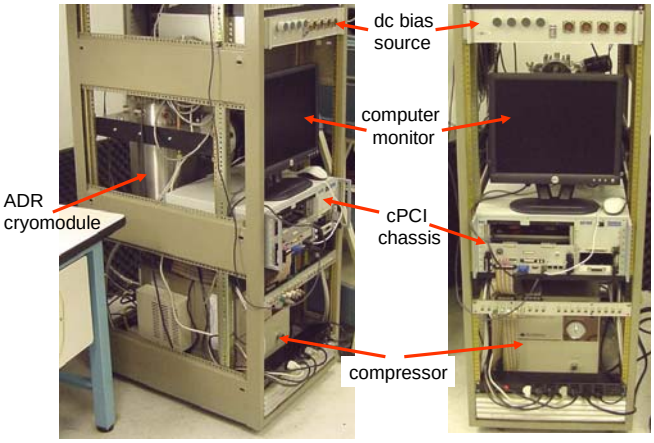

Fig. 4 Photo of the cryopackaged ADR test setup using commercial Sumitomo cryocooler mounted into the lower part of standard 19-inch rack.

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