Design and Operation of RSFQ Circuits for Digital Signal Processing

(Invited)

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Abstract - We have developed and experimentally evaluated at high-speed a complete set of arithmetic circuits (multiply, add, and accumulate) for high-performance digital signal processing (DSP). These circuits take advantage of the unique features of the Rapid Single-Flux Quantum (RSFQ) logic/memory family, including fusion of logic and memory functions at the gate level, pulse representation of clock and data, and the ability to maintain intercell propagation delays using Josephson transmission lines (JTLs). The circuits developed have been successfully used in the implementation of a serial radix 2 butterfly, a decimation digital filter, and of an arithmetic unit for digital beamforming.

I. Introduction

A. Why Superconductive DSP Now

Digital superconductive electronics can be inserted into digital signal processing systems sooner than into any other digital application. Superconductivity can offer solutions for a number of DSP problems which cannot be solved by semiconductor electronics. One of the most important among these is the ever-increasing demand on circuit throughput. Another is low-power processing, which is essential for many critical DSP applications with cooled front-end devices. Furthermore, future applications of superconductor analog-to-digital converters (ADCs) with performance unattainable by semiconductor counterparts will inevitably make the use of superconductor DSPs even more advantageous.

From a design point of view, a great variety of DSP algorithms allows us to choose the most suitable algorithm for the current maturity level of superconductor technology.

B. RSFQ-Based DSP: Merits and Challenges

Superconductive RSFQ digital technology [1] possesses a number of features making RSFQ-based DSP implementations extremely attractive.

1) High Throughput

The high throughput capability of RSFQ circuits is especially valuable for DSP implementations. Since this capability is even greater than currently required for some applications, it allows us to use a single bit-wide serial processing architecture. This enables the required functional complexity with much less hardware, thus bringing it within reach of present-day superconductive technology. With an increasing maturity level, parallel DSP implementations will be used when higher throughput is necessary.

2) Low Power

Extremely low-power dissipation enables high-density, compact packaging at the chip level. Low-level SFQ data and clock signals allow us to avoid any detrimental digital noise effects in mixed-signal circuits, e.g. the integrated high-sensitivity ADC front-end with decimation digital filter.

3) Internal Gate Memory

The internal memory of RSFQ gates allows the implementation of pipelined arithmetic modules using fewer gates. The basic RSFQ gates are essentially combinations of sequential and combinational gates which perform more complex logic functions than traditional semiconductor counterparts. This results in a significant reduction of the circuit complexity.

4) Flow Clocking

The physical identity of clock and data SFQ pulses along with the synchronous nature of the majority of RSFQ gates makes distributed flow clocking advantageous, and probably the only possible method at multi-GHz speeds. The use of JTLs provides predictable and controlled delays for clock and data transfer between gates. SFQ flow synchronization allows us to avoid the requirement of a high-power external clock since an SFQ clock is generated on-chip.

On the other hand, issues that make RSFQ DSP development challenging are: (1) the non-traditional set of basic cells requires a departure from the established design methodology; (2) unambiguous circuit testing at frequencies beyond 2 GHz is not trivial; (3) the use of JTLs for implementation of circuit flow timing increases circuit design complexity.

In this paper, issues of RSFQ DSP design and testing methodologies are addressed and the latest results of DSP RSFQ implementations are presented.

II. Design Methodology

A. Basic Set of RSFQ Elementary Cells

One can follow traditional design methods using RSFQ Boolean cells. However, this would lead to excessively complex and cumbersome circuitry. Since RSFQ gates are natural flip-flops, it is more advantageous to build a basic circuit set around T and RS flip-flops and their modifications. These modifications include adding destructive (DRO) and non-destructive (NDRO) readouts, as well as confluence input buffers. As a result, the functions of our basic cells are essentially the common DSP elementary operations of add, accumulate, and multiply.

Details of design and experimental evaluation of the most of these cells were described earlier. A T flip-flop with DRO and confluence buffer (FA-cell) performs the function of half or full addition [2]. A T flip-flop with NDRO and confluence buffer (ACC-cell) performs the function of an accumulation [1]. An RS flip-flop with NDRO (NR-cell) performs the function of multiplication [3], [4]. Since all these cells have an internal memory, they provide latching of their inputs or outputs. As elementary latch, an RS flip-flop (DR-cell) is used. For implementation of serial addition, an entire carry-save serial adder (CSSA-cell) was designed as a very effective single elementary cell, demonstrating the capabilities of a "non-Boolean" design approach [5].

A similar set of basic RSFQ cells is being successfully used by other authors [6]. A more traditional approach of composing DSP elementary functions using RSFQ Boolean cells and flip-flops is described in [7].

B. RSFQ DSP Functions

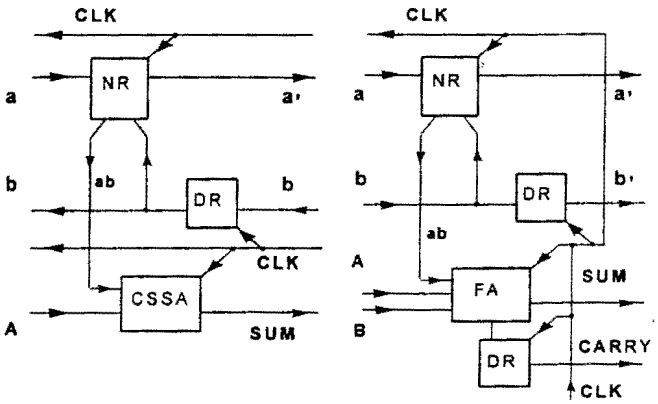
The most common DSP functional *primitive* is $X = WY + Z$. In order to perform this function, multipliers and adders are required. Figure 1 shows single-bit modules for serial and parallel implementations of multipliers. These modules are designed using the basic set of RSFQ cells described above. The cells are interconnected with JTLs providing SFQ pulse amplification and setting the necessary delays within the modules.

An entire serial multiplier module comprises 48 Josephson junctions (JJs) and dissipates only 13 μW of power [8]. A parallel multiplier module (PMM) employs 67 JJs and dissipates 19 μW of power.

C. Timing

In contrast to semiconductor logic or superconductive latching logic, the SFQ clock propagates similarly to data along JTLs. This feature of SFQ clock is especially suitable to the pipelined architectures common in DSP applications. It allows us also to "pipeline" the clock, i.e. a few clock SFQ pulses can simultaneously propagate along the circuit. The mutual direction of clock and data can be opposite (counter-flow timing) or the same (con-flow timing) [1]. Two types of con-flow timing can be employed: (1) data propagates faster than clock - one clock pulse drives data along an entire pipeline; (2) data propagates slower than clock - n clock pulses are required in order to perform the same function.

The clocking style should be selected according to the application. The choice is critically important for the best balancing of performance and layout feasibility. For example, in the design of a serial multiplier [8], both counter- and con-flow (data faster than clock) timing schemes were used simultaneously. Some authors prefer exclusively con-flow timing [9].



(a) (b)

Fig. 1 Block diagrams of single-bit modules of (a) serial multiplier; (b) parallel multiplier (PMM).

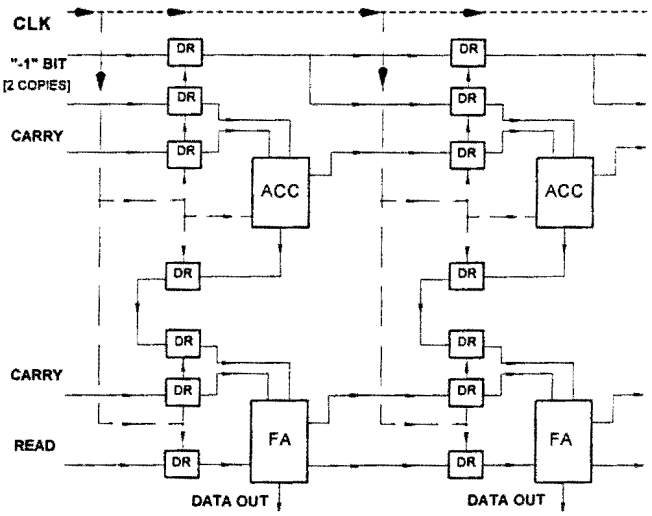


Fig. 2 Block diagram of a 2-bit fragment of the decimation digital filter for a 20 GHz operation.

In 2-D arrays of parallel multipliers [3] or decimation digital filters (Fig. 2), timing design becomes more complex. For parallel multiplier arrays, counter-flow, wave clock propagation controlled by coincidence junctions

circuits [3] seems to be preferable. However, its layout realization is quite difficult.

For the decimation digital filter of a high-resolution ADC [10], we have chosen *broadcasting* con-flow (clock faster than data) 2-D timing design (Fig. 2). In this design, a fast master clock propagating along a single horizontal JTL triggers SFQ clock propagation in the intermodule vertical clock lines. In order to make the intermodule timing completely independent, a number of latches (DR-cells) are introduced. The target design clock frequency is 20 GHz. The master clock delay has to be smaller than any data delays between adjacent modules.

III. Test Methodology

A. On-Chip Test Systems

On-chips test systems are essential for testing of high-speed RSFQ circuits. We have developed two different on-chip test systems. The Logic Tester/SFQ Sampler [2] is used mainly for functionality verification at low clock speed but with an ability to set picosecond delays between SFQ pulses of different inputs. Figure 3 demonstrates the results of correct operation of a parallel multiplier module using this Logic Tester. Some limited high-speed sampling tests can be performed using this on-chip test circuitry.

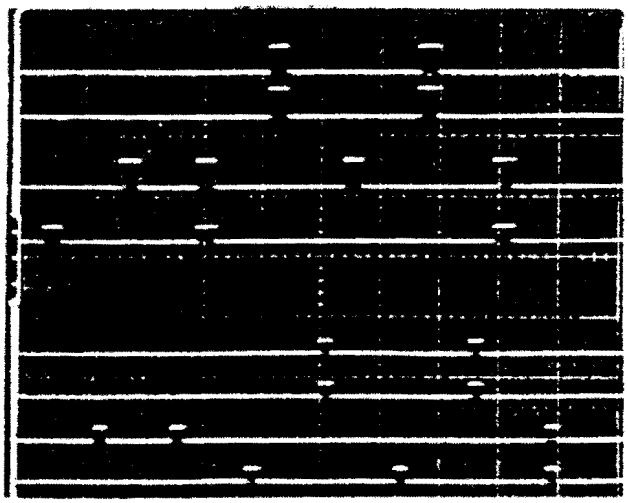
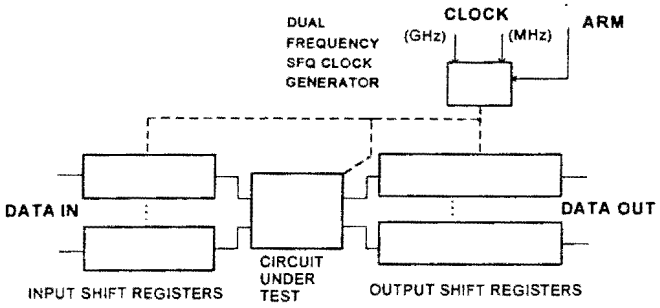
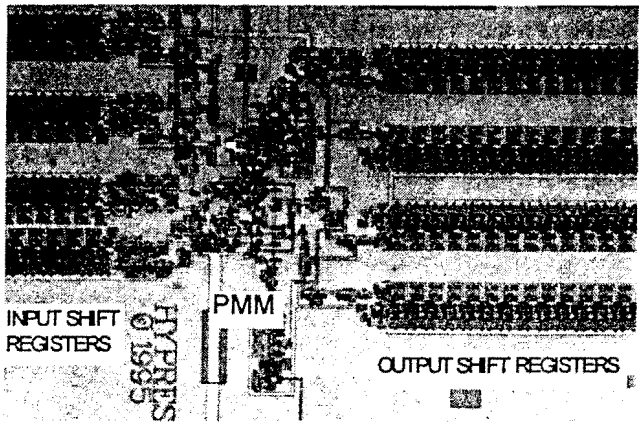


Fig. 3 Correct operation of a parallel multiplier module imbedded in the Logic Tester. The top 4 traces (from top to bottom) are the ***a***, ***b***, ***A***, and ***B*** inputs. The bottom four traces are outputs ***a'***, ***b'***, ***SUM***, and ***CARRY***.

The true unambiguous high-speed test at frequencies beyond 2 GHz can be conducted using the on-chip shift register-based test system. The block diagram of this circuit is shown in Fig. 4a. The layout of this system with a parallel multiplier module as a circuit under test is presented in Fig. 4b. The test system consists of a dual



(a)



(b)

Fig. 4 (a) Block diagram of the on-chip shift register-based test system. (b) Layout of the RSFQ parallel multiplier module (PMM) inserted in this test system. The horizontal layout size is 1.7 mm.

frequency clock generator, a set of the input shift registers to load input patterns, and a set of the output shift registers to capture output data at high speed, store it, and then off-load it to room temperature electronics at low-speed.

1) Loading of Input Patterns

The clock generator produces low-speed (MHz) SFQ clock pulses to provide loading of input shift registers with input patterns.

2) High-Speed Operation

The high-speed (GHz) SFQ clock is triggered by an externally generated continuous sinewave. The challenge here is to enable only a certain number of high-speed SFQ pulses equal to or less than the length of the output shift registers. Normally, we use an externally generated short (~ ns) **ARM** pulse to open the RSFQ switch. This pulse is generated by subtraction of two skewed longer pulses. For fine adjustment of its edges, a mechanical delay line is used. Recently, we have developed an RSFQ clock-controller for the direct counting of high-speed SFQ clock pulses.

3) Off-Loading of Output Data

The clock generator produces low-frequency (MHz) clock pulses to read out the data captured from the output shift registers. Usually, we design the length of the output

shift registers to be larger than required in order to make the choice of the width of enabling external pulse less critical. This shift register-based test system has been successfully tested up to 14 GHz.

B. Examples of Recent Test Results

Figure 5 shows the high-speed test results for the PMM on a shift register-based test chip. A 2.5 MHz clock is used to load and off-load the data. The **SUM** and **CARRY** outputs are identical to those shown in Fig. 3 for low speed, except they are in a non-return-to-zero (NRZ) format. These results show the multiplier module operating at 5.3 GHz. Partial operation (ab + B) was observed up to 13.7 GHz.

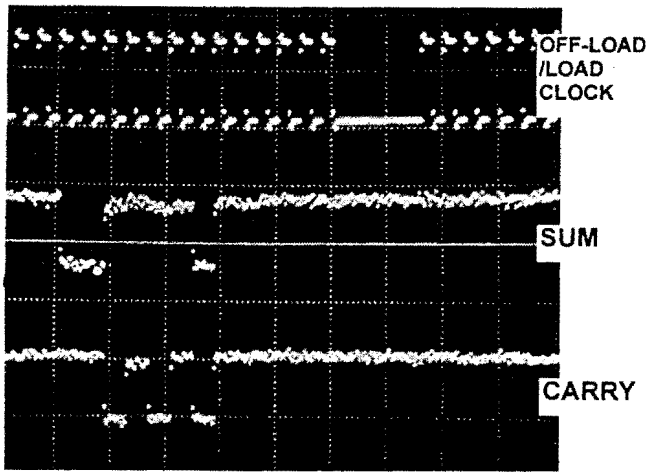


Fig. 5 Correct operation (ab + A + B) of the parallel multiplier module with the shift-register test system at 5.3 GHz (load/off-load clock is 2.5 MHz). The input data is identical to that in Fig. 3. The outputs (in an NRZ format) are inverted by a GaAs amplifier. The vertical scale for the outputs is 2 mV/div. The horizontal scale is 500 ns/div.

A similar test system has been successfully used to demonstrate the successful operation of an 8-bit serial multiplier up to 6.3 GHz [8].

The DSP circuits developed are being used for the implementation of various DSP chips. We have successfully implemented the operational FFT radix 2 butterfly circuits using serial RSFQ arithmetic [8]. The parallel arithmetic is being used for implementation of multiplier-adder chips for digital beamforming. Digital decimation filters for high-resolution ADCs using RSFQ accumulator-adder circuits are also being tested.

IV. Conclusion

The use of a basic set of RSFQ elementary cells based on flip-flops rather than on combinational gates leads to the development of efficient and compact DSP functions of multiply, add, and accumulate.

Flow timing of RSFQ circuits has proven to be practical in the implementation of relatively large DSP circuits. The choice of concrete flow-timing scheme depends on the applications. The proper choice of a timing scheme leads to maximization of operating speed and to reducing of the layout burden of extra JTLs used for clock distribution.

Unambiguous RSFQ circuit testing at frequencies above 2 GHz has been demonstrated using an on-chip shift register-based test system. This system enables circuit test at full GHz speeds while communicating with semiconductor electronics at low speed.

Finally, we have designed, fabricated, and evaluated at high-speed an RSFQ library of multiply-add-accumulate elements with high throughput suitable for the implementation of a variety of DSP processors. To our knowledge, our 6.3 GHz serial multiplier and 13.7 GHz module of parallel multiplier are the fastest DSP circuits to date.

Acknowledgment

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