Digital RF Receiver Systems

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***Abstract*—High speed of superconductor RSFQ electronics allows the implementation of digital radio frequency (RF) receivers capable of direct digitization of high frequency (up to tens of GHz) RF signals. The key element of such Digital-RF receivers is a high sampling rate analog-to-digital converter (ADC) capable of direct conversion of RF input to the digitized RF data stream with high fidelity. These data streams can be then processed by high speed RSFQ digital circuits performing various digital signal processing functions (RF DSP). We demonstrated several single-chip Digital-RF receivers consisting of ADC modulators and RF DSPs cryopackaged using commercial 4K close-cycle refrigerators and performing various tasks of signal acquisition, datalink and satellite communications. The Digital-RF receiver 4K Nb chips can be integrated with 70K high-temperature superconductor analog filters, low-noise amplifiers as well as 300K semiconductor interface and data processors into a single hybrid-temperature hybrid-technology $(ht)^2$ system. In this report, we review the progress in the development of new ADCs and cryogenic system integration.**

I. INTRODUCTION

Digital-RF technology is a disruptive technological innovation capable of changing wireless communications, radar, and surveillance system architectures dramatically. Practical results have been achieved in proving that superconductor Digital-RF technology can be applied to such systems altering the way these systems have been traditionally built. In these systems, fundamental advantages of superconductivity translate into system benefits through enabling direct digital processing of wide band, high radio frequency (RF) signals and expanding digital domain throughout the entire system. The availability of relatively small 4K cryocoolers has lowered the foremost market barrier for cryogenically-cooled digital electronic systems.

HYPRES has developed and delivered several cryocooled superconductor Digital-RF receiver systems directly digitizing signals in a broad range from kilohertz to gigahertz, operating with live satellite signals in X-band and performing signal acquisition from HF to L-band with ~30 GHz clock [1].

II. PROGRESS IN ADC DEVELOPMENT

In order to increase Digital-RF receiver dynamic range, we are pursuing higher order and multi-threshold ADC modulator designs.

Manuscript received 15 May 2009. This work was supported in part by the Office of Naval Research and US Army CERDEC.

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A. ADC with Higher-order Modulator

Multiple feedback loops are normally required for the implementation of higher order ADC modulators. However, delays in the feedback loops might pose a design challenge for higher order modulators. Recently, we have developed a modulator with two implicit feedback paths exhibiting a quasi-instantaneous feedback by connecting two resonators directly to the comparator.

The RF input was split and applied through inductive coupling to each resonator. In addition, a SQUID amplifier stage was used to connect two LC resonators in series to get the desired loop filter transfer function. We implemented and measured a two-implicit-loop band-pass ΔΣ ADC chip (Fig. 1). A 1:16 deserializer was integrated on the same chip to reduce output data rate. We observed the desired noise-shaping despite the data acquisition system limiting f_{clk} to about 10 GHz, and therefore, the maximum SNR [2].

It is easier to scale such a multiple implicit feedback ADC design to higher order. Furthermore, the quasi-instantaneous feedback allows higher freedom in choosing clock frequencies compared to the one with explicit feedback. However, the same quasi-instantaneous feedback feature is problematic for higher RF frequencies due to imprecise timing in implicit feedback. Therefore such an ADC design is preferable for relatively low RF frequencies, e.g. UHF.

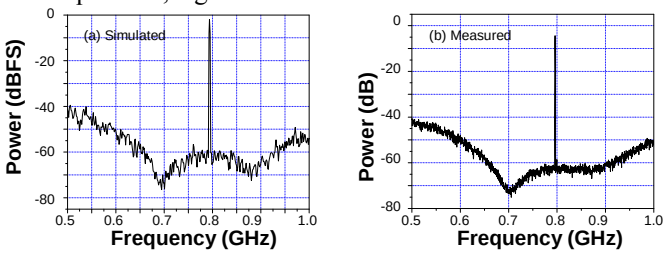

Fig. 1. Two-implicit-loop ADC: (a) Simulated and (b) measured spectra of ΔΣ modulator used to digitize a 200 MHz band around 800 MHz. The 5-mm ADC chip included a 1:16 deserializer and was clocked at 10.24 GHz. The input signal frequency is 796 MHz. The measured SNR is 31.6 dB in 660-915 MHz band.

B. ADC with Multi-threshold Quantizer

One can extend the ADC signal-to-noise ratio by increasing the number of thresholds in the quantizer. This leads to higher circuit complexity for both the modulator and subsequent digital signal processing circuitry.

In order to avoid the necessity of precision component matching and/or error-correction processing for mitigation of nonlinear distortions, we employ a parallel combination of Josephson junction comparators, together with a sequence of

magnetic flux bias levels, to yield an automatic cyclic permutation of the quantization levels. The thresholds are spread uniformly between 0 and Φ_0 by applying an appropriate flux bias in each arm. For N comparators, there are N thresholds separated by Φ_0/N. For a given input signal level, k comparators will switch, each sending back a feedback signal of Φ_0, and causing a $k\Phi_0/N$ shift of flux bias. This multiple switching serves to randomize small mismatches in bias and element values, reducing nonlinear distortions.

In a Digital-RF receiver, the ADC modulator is followed by a digital channelizer circuit comprising in-phase and quadrature (I&Q) mixers and two decimation filters with appropriate output drivers [1]. The multi-threshold ADC implementation requires the digital mixer with multi-bit input and a summing circuit to add all the N individual comparator outputs into a multi-bit binary word for input to decimation digital filters (DDFs). We have implemented a Digital-RF receiver chip with two-threshold ADC, 2x1 digital I&Q mixer, and two DDFs. This circuit was measured to produce 63 dB SFDR and 41 dB SNR in 96 MHz instantaneous bandwidth (Fig. 2) [2].

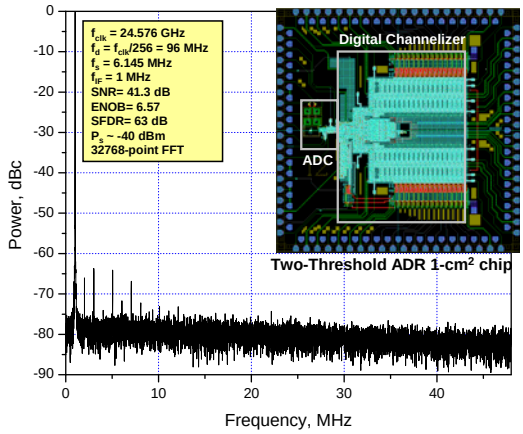

Fig. 2. One half of the digitized spectrum (from one digital filter) of a two-threshold receiver (ADR) chip. The output I and Q data rates are 96 MSample/s corresponding to decimation ratio of 256.

III. System Integration and Demonstration

Several Digital-RF receiver demonstration systems were assembled to perform various applications of satellite communications, datalink, and signal intelligence (SIGINT). These systems were constructed following the hybrid-temperature hybrid-technology (ht^2) approach [1] of integrating different functional blocks co-located at different temperature stages and implemented with different technologies. Compared to the first ht^2 Digital-RF systems [1], [3], we have further improved their modularity and robustness. In particular, the system cryopackage has been modularized to permit replaceable 4K cryomodules to house different size chips depending on application. This allows a single system to be used for different applications by simple replacement of the 4K cryomodules (Fig. 3).

Fig. 4 shows recent demonstration of such Digital-RF system, which comprised a 4K cryomodule with 5x5mm^2 Nb chip with an L-band band-pass ΣΔ ADC and RSFQ 1:16 deserializer. The RF input was routed via 70K high-temperature superconductor (HTS) filter built by University of Waterloo. The digital output was connected to the 300K FPGA processing module. This system performed multinet operation with two datalink hopping networks.

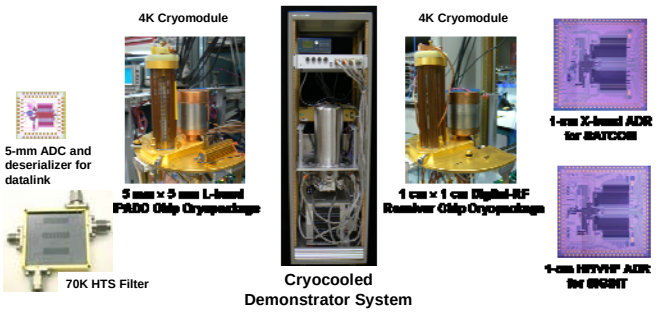

Fig. 3. Rack-mounted cryocooled Digital-RF receiver system (center) and its main replaceable 4K cryomodules for 5x5 mm^2 (left) and 10x10 mm^2 chips (right). The HTS analog filters are mounted on a 70K stage.

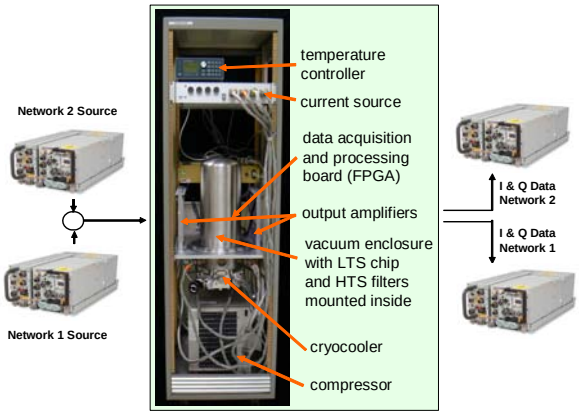

Fig. 4. The multinet datalink system. The ht^2 Digital–RF receiver system is based on 70K HTS analog filter and 4K RSFQ wide-band L-band ADC and deserializer, and 300K FPGA processor. Two hoping networks were simultaneously received, dehopped, and demodulated.

IV. Conclusion

Direct digitization of wide-band RF signals requires ADCs with high dynamic range. We are improving the ADC dynamic range by utilizing multiple feedback loop schemes and multi-threshold quantizers. Single-chip digital receivers, combining ADCs with digital processing circuits and integrated into the modular ht^2systems have demonstrated to perform various tasks of satellite communications, multinet datalink, and other applications.

Acknowledgment

We thank HYPRES foundry team for chip fabrication and team of Prof. R. Mansour of University of Waterloo for providing HTS filters.

References

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