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A novel way of digital information processing in the Josephson junction circuits

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A complete system of logic and memory elements based on the Josephson effect is demonstrated, with both information and timing signals presented by single voltage pulses V(t) with area $\int V(t)\,dt$ close to magnetic flux quantum Φ_0. The major advantages of the new system are discussed including dc-power supply, ultrashort cycle time and wide parameter margins

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1. All reported Josephson logic systems are based on two ways of physical representation of the digital information.

In the first way, the information is coded by the magnetic flux trapped in superconducting loops; presently the single flux quanta $\Phi_0 = h/2e \approx 2.07 \cdot 10^{-15}$ Wb are used in most devices [1-8]. The basic drawback of this representation is that the magnetic flux suffers a nonvanishing drop along even a superconducting transmission lines. As a result, the information coded in this way can be transferred practically to few neighboring logic cells during a single clock period. This property is hardly compatible with the traditional computer architectures [7].

The second way, the information representation by the voltage V across the Josephson junction is used in most resent developments of the superconducting logics [9-11] being compatible with the traditional architectures. Its major disadvantage is that the time $\tau_{R \to S}$ necessary for the juction reset from its resistive (R) to superconducting (S) state is rather large (up to 1 ns [12]) so that the minimum clock period ($\tau_C = \tau_{S \to R} + \tau_{R \to S}$) turns out to be large than that of the modern semiconductor gates [13].

The purpose of the present work is to demonstrate the possibilities of another way to represent digital information in the superconductor electronics. In this way the information is stored in the form of single flux quanta, but is transferred in the form of single voltage pulses of the area

$$\int V(t)\, dt = \Phi_0 \quad . \qquad (1)$$

In contrast with the earlier proposals [4-7] to use such pulses in logic circuitry, we present the logic unity (zero) by presence (absence) of the pulse during a period between two consequent timing (T) pulses. The latter pulses are similar in area (1) and shape with the signal ones, but are transmitted along the separate lines.

2. As a simple illustration of our principles, consider a circuit (Fig. 1) performing the Boolean function $F = ((\overline{A + B}) + C) \cdot D$. The circuit consists of gates NOT, OR, AND interconnected by buffer stages. Each gate has signal inputs S_i and a timing input T, all inputs are supplied by the single voltage pulses (1). Signal pulses can change the internal state of the gate, independently of the exact time of their arrival (within the given period between the timing pulses). The latter pulse reads out the resulting internal state of the gate, i.e., induces a single pulse of the same area (1) at the gate output in the case when the performed logic function is equal to unity.

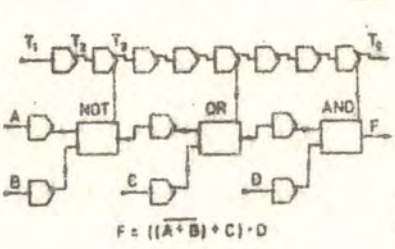

Figure 1.

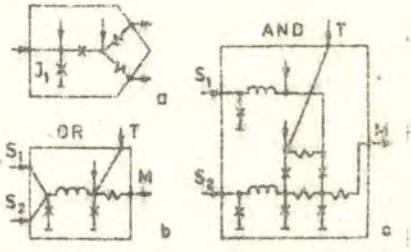

Figure 2.

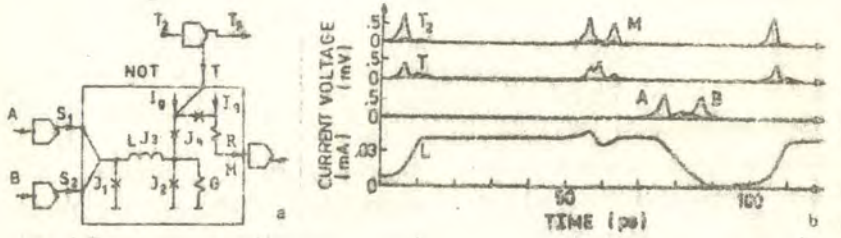

Figure 3.

3. Figures 2 and 3 show possible structure the components of the above circuit (Fig. 1). The buffer stages(Fig. 2a) is closed to those discussed earlier [7]; they provide unilateral transfer of the pulses (1) between the logic gates, with the simultaneous regeneration of the pulses. The regeneration is provided by dc-biased non-hysteretic (low - β_c) Josephson junction J_1, which performs a 2π - leap of its phase ϕ triggered by an input pulse. Series connection of the buffer stages forms a neyristor-type transmission line capable to transfer information to unlimited distance along an integrated circuit with the velocity approaching that of light. Information multiplication is readily arranged and channeling of pulses from two lines to one can be provided by simple connection of the similar buffer stages.

Figure 2b shows that the logic gate OR can be designed on the basis of a symmetrical two-junction superconducting quantum interferometer flux-biased by $\Phi_0/2$ and hence possesing two similar stable states. An input pulse S_1

arriving first in time changes the initial state of the interferometer while the following signal pulse (if come) does not change this state. The timing pulse resets the initial state thus preparing the gate to the new operation period. This back switching induces a similar voltage pulse at the gate output, presenting the logic unity. Such a pulse doesn't arise in the absence of the signal pulses S_i so that the OR function is really performed.

Figure 3a shows a possible structure of the NOT gate which is typically a bottle-neck in all Josephson junction logics. The gate consists of the interferometer similar to discussed above accompanied by the buffer stage (J_3, J_4, R) and the additional shunt conductance G ; the latter circuit element reduces considerably the effective I_cR product of the junction J_2 . The timing pulse triggers the 2π - leap of the phase of one of the junctions J_2 , J_3 depending on the state of the interferometer. As one can get convinced by the simulation results† presented in Fig. 3b the difference in the I_cR products of the junctions results in the pulse of the output buffer stages only if the junction J_3 has been switched. Our analysis has shown that the circuit presented in Fig. 3a can also be used as a two-argument OR-NOT (i.e. NOR) gate, which alone is sufficient to compose an arbitrary logic circuits. It can be more convenient, however, to use also some other logic gates such as OR (Fig. 2c) and AND (Fig. 2d).

All the circuits considered are logic flip-flops rather than mere gates, so that they can be directly employed to design various memories (including associative ones) as well as sequential switching circuits.

4. The new general principle of the digital information processing makes possible a drastic improvement of the Josephson-junction computing.

Firstly, the total time period per a logic operation including the gate reset (see plots in Fig. 3b) can be only factor of 5 to 10 longer than the single Josephson junction pulse time. As the result, the operation frequency of the logic circuits with quite ordinary externally-shunted Josephson junctions (Nb - NbO_x - Pb ; $j_c = 10^3$ Amp/cm^2; $S = 10$ μm^2; $I_c = 0.1$ mAmp; $\beta_c = .7$; $I_cR = 0.3$ mV) can be as high as 30 to 100 GHz, i.e., factor 10^2 faster than that of the resistive logics [10]. Employing the modern edge-type high-current-density junctions with $\beta_c < 1$ (see, for example, revue [14]) without external shunting allows one to increase the operation frequency by one more order of magnitude.

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† $I_{c1} = I_{c2} = 45$ μAmp; $I_{c3} = 70$ μAmp; $I_{c4} = 35$ μAmp; $I_g = 25$ μAmp; $I_cR = 1$ mV; $G = 0.08\ \Omega^{-1}$; $L = 60$ pF; $R = 2\ \Omega$; $\beta = 0.7$

Secondly, the physical similarity of the signal and timing pulses enables one to arrange the local generation and logic processing of the timing pulses using the similar logic circuitry. As a result, one can abandon the idea of the clock general for the whole processing device, limiting oneself to the local timing for each its fragment. In the same time, presence of the timing pulses make the mutual synchronization of any parts of the computer readily attainable.

Lastly, according to our simulations using the COMPASS program [15], all the circuits discussed have critical current margins as large as at least ± 20 %. This large tolerance for the parameter scattering gives every hope that basic logic gates operating according the new principle will be realized experimentally in the nearest future, so that construction work on the larger digital devices could be started.

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References

1. T.A. Fulton, R.S. Dynes and P.W. Anderson - Proc. IEEE, vol. 61, p. 28, 1973.

2. K.K. Likharev - IEEE Trans. Magn., vol. MAG-13, p. 245, 1977.

3. K. Nakajima and Y. Onodera - J. Appl. Phys., vol. 47, p. 1620, 1976.

4. K.K. Likharev - Radiotekhn. i Elektron., vol. 19, p. 1494, 1974 (Radio Engineering and Electron. Phys).

5. J.P. Hurrell, D.C. Pridmore-Brown and A.H. Silver - IEEE Trans. E. D., vol. ED-27, p. 1887, 1980.

6. C.A. Hamilton, F.L. Lloyd - IEEE E. D. Lett., vol. EDL-3, p. 335, 1982.

7. G. Oya, M. Yamashita and Y. Sawada - IEEE Trans. Magn., vol. MAG-21, No. 2 , 1985 (in ASC-84).

8. K.K. Likharev, S.V. Rylov and V.K. Semenov - IEEE Trans. Magn., vol. MAG-21, No. 2 , 1985 (in ASC-84).

9. Y. Hatano, T. Nishino, Y. Tarutani and U. Kawabe - Appl. Phys. Lett., vol. 44, p. 1095, 1984.

10. J. Sone, T. Yoshida and H. Abe - Appl. Phys. Lett., vol. 40, p. 741, 1982.

11. H. Nakagawa, T. Odake, E. Sogawa, S. Takada and H. Hayakawa - Jpn. J. Appl. Phys., vol. 22, p. L297, 1983.

12. T.A. Fulton - Appl. Phys. Lett., vol. 19, p. 311, 1971.

13. P.M. Solomon and H. Morkoç - IEEE Trans. E.D., vol. ED-31, p. 1015, 1984.

14. R.A. Buhrman - Physica, vol. 126 B+C, p. 62, 1984.

15. V.K. Semenov and V.P. Zavaleev - IEEE Trans. Magn., vol. MAG-21, No. 2, 1985 (in ASC-84).