RSFQ Logic/Memory Family: A New Josephson-Junction Technology for Sub-Terahertz-Clock-Frequency Digital Systems

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Invited Paper

Abstract—**Recent developments of the rapid single-flux-quantum (RSFQ) circuit family are reviewed. Elementary cells of the family can generate, pass, memorize, and reproduce picosecond voltage pulses $V(t)$ with nominally quantized area $\int V(t)\,dt = \Phi_0$, corresponding to transfer of a single magnetic flux quantum $\Phi_0 = h/2e$ across a Josephson junction. Functionally, each cell can be viewed as a combination of a logic gate and an output latch (register) controlled by clock pulses, which are physically similar to the signal pulses. Hand-shaking style of local exchange by the clock pulses enables one to increase complexity of the LSI RSFQ systems without loss of operating speed. The simplest components of the RSFQ circuitry have been experimentally tested at clock frequencies exceeding 100 GHz, and an increase of the speed beyond 300 GHz is expected as a result of using an up-to-date fabrication technology. The review includes a discussion of possible future developments and applications of this novel, ultrafast digital technology.**

I. Introduction

SEMICONDUCTOR microelectronics continues its victorious march, despite repeated claims of finding new physical principles that would allow one to process the digital information more effectively (faster, cheaper, etc.) than one could with the semiconductor-transistor-based integrated circuits. Most of these claims are justly criticized for their insufficient account of requirements imposed by the computer architectures and LSI fabrication technologies.

Even the most ardent proponents of the semiconductor digital technologies agree, however, that quite a serious challenge for them has come from the superconductor integrated circuits based on the Josephson effect. (For an excellent introduction to the effect, as well as to the superconductor electronics as a whole, see [1].)

The basic common features of all Josephson-junction technologies, favorable for their digital applications, are as follows:

i) Effective impedance R_{ef} of a Josephson junction as a waveform generator can be readily adjusted to that (ρ) of the superconducting microstrip line (typically $\rho \cong 10\ \Omega$). Such lines, with their very low attenuation and dispersion, allow one to pass picosecond waveforms for distances well exceeding the typical chip size [2], with a low crosstalk. As a consequence, ultrafast digital signals can be passed along the chips ballistically (rather than diffusively) with a propagation speed $\bar{c}$ approaching that of light. (It is a pity that so many advertisers of the optoelectronics forget that one does not need to have *light* for having the *speed of light*!)

ii) The signal voltage amplitude V in the Josephson junction circuits does not exceed the value $2\Delta(0)/e$ established by the energy gap $\Delta(T)$ and equals ~ 3 mV for the traditional low-T_c superconductors (we will discuss prospects arising from the discovery of the high-T_c superconductivity in Appendix III). As a result, the power $P \cong V^2/R_{ef}$ dissipated by a Josephson junction even in its "open" (resistive) state is typically below one microwatt. Hence the problem of the heat removal from VLSI circuits is either trivial or at least quite solvable. This fact leads to the possibility of the close packaging of the superconductor-circuit chips, with the corresponding decrease of time delays for the interchip communication.

iii) Intrinsic switching speed of the Josephson junction is also very high, typically few picoseconds (switching delays as low as 1.5 ps have been demonstrated recently [3]).

iv) Lastly, the Josephson junction fabrication technologies are considerably simpler than those of the present-day semiconductor (both Si and GaAs) transistors with similar design rules. Physical limits of the junction size ($a \gtrsim 0.1\ \mu$m) are also close to those of the semiconductor transistors and can hardly be regarded as a serious problem at the present-day patterning techniques.

Small wonder, then, that the famous project of the IBM Corporation aimed at creation of a prototype Josephson-junction computer attracted so much attention in the 1970's and early 1980's (for a detailed description of the project the reader is referred to the special issue of *IBM J. Res. Devel.* [4]; several important results have been reported later [5], [6]; see also [7]). When the attempt was eventually dropped in late 1983, the news produced a major sensation in the electronics world.

Now, after a few years we believe to have a basically clear view of the main reasons for this failure. Most important, a need in liquid-helium cooling of the whole system was *not* the main reason. In fact, modern refrigeration techniques do justify commercial production even of instruments like SQUID's [8] and reflectometers [9] which use very simple superconductor IC chips with just a few Josephson junctions. For possible LSI/VLSI circuits the refrigeration costs would be far from being the major concern.

The first real drawback of the IBM project was utilization of

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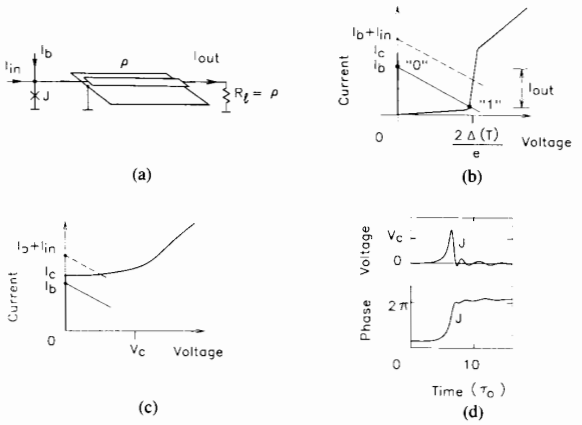

Fig. 1. The simplest stage of the Josephson junction logics. (a) Equivalent circuit and schemes of its operation when using (b) an underdamped and (c), (d) overdamped junction. Plots in Fig. 1(d) and all similar plots below were obtained by numerical simulation of the circuit dynamics within the RSJ model ($\beta_c = 1$) of the junctions [11] using the PSCAN program [34]. Inputs and outputs of the circuits were supposed to be connected to the standard RSFQ buffer stages (see below).

"soft" superconductors like lead alloys. The temperature recycling of the devices between 300 K and 4.2 K leads to a gradual degradation of ultrathin (2–3 nm) oxide layers used as the tunnel barriers in the Josephson junctions (because of recrystallization of the electrode films) and eventually to an unacceptable change of their parameters. Despite a drastic improvement of such materials achieved in the course of the IBM project, they have presumably never approached a desired stability.

The second, and probably the main, reason for the IBM project failure was an unfortunate choice of the logic circuitry. The superconducting technologies still lack a practical transistor, and should use active two-terminal devices instead. Fig. 1(a) shows a simplified but conceptually correct version of the simplest logic gate, the buffer stage, used in the IBM-type logics. It employs a tunnel Josephson junction (J) that is naturally underdamped and thus exhibits a hysteretic dc *I-V* curve (Fig. 1(b), biased by a dc current I_b slightly less than its critical value I_c. Initially the junction is in its superconducting state ($V = 0$, point "0" in Fig. 1(b)). An arriving signal current I_{in} drives the total junction current beyond I_c, and induces its switching to its resistive state "1" with $V \neq 0$, so that a considerable part I_{out} of the current is steered into the load R_l (typically, through the microstrip line with the wave resistance $\rho \simeq R_l$); the latter current serves as an output signal. (In most implemented versions of this logic [22], the current I_{in} is also used to *suppress* I_c simultaneously, but this fact changes nothing essential in our qualitative discussion.) This is the "0"→"1" switching process, which can be very fast (few picoseconds).

Note, however, that the reset (the "1"→"0" switching) cannot be achieved by merely turning the signal I_{in} off; the circuit remains in its "1" state. (Due to this property, such logics have been nicknamed *latching*.) The only practical way to reset the gate to its "0" state is to switch off the bias current I_b. In the latching logics, this periodic reset of all gates is achieved by using RF rather than dc current supply of all the gates; this waveform performs also a global synchronization of the whole device. Unfortunately, this operation mode has severe drawbacks:

i) The necessary supply of power per gate is well beyond that of the signal which can be produced by a similar gate. Thus the clock signals should be generated externally, so that the latching circuits are restricted to external global timing. As a result, their flexibility for system design is rather limited (see, e.g., [10]).

ii) A practical generation of the necessary rf supply presents rather a problem. In fact, its current amplitude per gate should be of the order of the critical current I_c, which cannot be made less than $\sim 100\ \mu$A in order to ensure operation stability with respect to the thermal fluctuations [1], [11] (see also Appendix 3). Thus, for a chip containing, say 10^6 gates, one would need the rf current with the amplitude ~ 100 A and source resistance $\sim 10^{-4}\ \Omega$. The only apparent way to induce RF currents so high is their on-chip or on-board transformation using special superconducting thin-film structures; the upper frequency of such transformers can be hardly raised beyond a few gigahertz because of their intrinsic resonance problems [12].

iii) A close limitation of the clock frequency of a latching logic comes from another source, an undesirable effect of the junction switching to the opposite resistive branch of its symmetrical *I-V* curve (Fig. 1(b)) during the decrease of the supply current. This so-called punch-through effect becomes noticeable at RF supply frequencies of the order of 1 GHz for typical Josephson-junction parameters (for details, see, e.g., sec. 5.3 of the monograph [11]).

Thus there have been no prospects found to increase clock frequencies of the latching-logic circuits beyond a few gigahertz. This speed is higher but comparable to those of the fastest GaAs digital circuits which do not require the helium refrigeration (see, e. g., [13]). This marginal advantage was found insufficient for a massive transfer to a completely new technology, and this was presumably the major reason to discontinue the large-scale IBM effort (the latching logics are also responsible for other technical problems, like a poor isolation of the logic gates).

This discouraging decision, however, has not terminated work on the Josephson-junction computing in other laboratories, and we can claim that *since 1983 both major problems outlined above have been solved in principle.*

The first contribution has come from Japan. Several laboratories including those of Fujitsu, Hitachi, NEC, and ETL united by the Japanese government project [14] have managed to improve the Josephson-junction fabrication technology using niobium rather than the lead alloys as the superconductors, and aluminum oxide instead of the indium oxide as the tunnel barrier material. As the result of utilization of these "rigid" materials, the thermal recycling has virtually ceased to be a problem [15]. The "niobium" technologies have been brought to a degree of perfection and make it feasible to fabricate the LSI circuits, in particular digital ones. For example, a 4-bit microprocessor developed by Hitachi [16] is a 2.5-μm design rule 5×5 mm^2 chip that contains 8454 Josephson junctions and 9027 resistors. Microprocessors of an almost similar complexity have also been developed by Fujitsu [17] and ETL [18]; moreover, Fujitsu recently announced [19] an 8-bit microprocessor containing about 22 000 Josephson junctions. Memory chips of nearly the same integration scale have been demonstrated by NEC [20] and ETL [21].

All these circuits, however, are based on the latching logics very similar to those employed in the IBM project (with some modifications, for a review see [22]). As a result, their operation speed remains low (on the Josephson junction time scale); for example, the maximum clock frequencies of all the microprocessors referred to above were close to 1 GHz. Such a speed can

hardly give superconductor digital electronics a decisive advantage over semiconductor technologies.

The purpose of this paper is to review a step toward a drastic increase of the operation speed of the Josephson junction digital circuits, developed since 1985 in Moscow by a joint team of the Moscow State University (MSU) and the Institute of Radioengeneering and Electronics (IRE). In 1985, Likharev, Mukhanov, and Semenov of MSU suggested [23] an entirely new approach to Josephson junction computing. In this approach, the binary information is presented not by the dc voltage (as in all semiconductor transistor logics, as well as in the superconductor latching logics), but by very short (picosecond) voltage pulses $V(t)$ of a quantized area:

$$\int V(t)\,dt = \Phi_0 \equiv \frac{h}{2e} \simeq 2.07\ \text{mV} \times \text{ps}. \qquad (1)$$

An essence of this idea is that these *single-flux-quantum* (SFQ) pulses (1) can be quite naturally generated, reproduced, amplified, memorized, and processed by elementary circuits comprising *overdamped* Josephson junctions. This unique ability, fully appreciated in some analog devices based on the Josephson effect [11] (see also Appendix II), was virtually neglected in the latching logics; moreover, in the latching logic circuits the SFQ pulse generation is an internal reason for the above-mentioned punch-through effect, which limits the operation speed.

The first version of the new logic/memory family relied heavily on ohmic resistors for interconnection of the Josephson junctions, and thus was nicknamed the *resistive single-flux-quantum* (RSFQ) logic [23]. During 1985–1986, the MSU team designed the first experimental chip containing the key elements of this version. By summer of 1986, the IRE group fabricated and tested the first samples. Somewhat unexpectedly for the authors, the circuit operated perfectly at clock frequencies up to 30 GHz [24], a factor of ~ 30 faster than any latching logic device and a factor of ~ 2 faster that any other digital device of a similar complexity tested to that date.

By that time it was recognized that the first (''resistive'') version of the RSFQ circuitry suffered rather narrow parameter margins. The second version [25], which used additional Josephson junctions (rather than the resistors) for the connections, allowed not only a drastic broadening of the margins but also a further increase of operating speed. It was called the *rapid single-flux-quantum* logic (to some extent, in order to save the original abbreviation RSFQ). Since then three test circuits containing the basic components of the new version have demonstrated their workability at clock frequencies in excess of 100 GHz with quite decent parameter margins [26]–[28], despite of a relatively primitive 5-μm (all-Nb) technology used for their fabrication. Numerical simulations show that transfer to a 1-μm technology can increase the speeds beyond the 300-GHz level. Even more important, a self-timing scheme for the RSFQ circuitry, which was suggested simultaneously [29], promises to extend these incredibly high operating speeds to digital systems of virtually arbitrary complexity.

These developments received considerable publicity in the Soviet Union but hardly any outside of that country. Nevertheless, we believe that a major success in such a big enterprise as bringing practical computer speeds close to the terahertz level can hardly be achieved without an extended international cooperation/competition. This review paper can be considered as our sincere attempt to attract attention of the international electronic engineering community to these remarkable prospects.

TABLE I
THE RSFQ TIME UNIT τ_0 (EQUATION (2)) AS A FUNCTION OF THE LINEAR SIZE a OF THE JOSEPHSON JUNCTION FOR THE Nb/Al-OXIDE/Nb TECHNOLOGY (FOR $I_c = 100\ \mu$A)

Junction size a, μm	5	2.5	1.25	0.7
Time unit τ_O, ps	4	2	1	0.5

The paper is organized to be ready for a piecemeal consumption. To those interested in the basic ideas alone, we recommend reading Section II, which describes the backgrounds of the RSFQ operation, a few initial sections of both Sections III (elementary RSFQ cells) and IV (examples of the RSFQ arithmetic), and then Section V (describing the self-timing concept), Section VI (prospects for system development), and concluding Section VII completely, skipping the Appendixes. On the other hand, the reader who studies the paper thoroughly will really be updated on the problem. In order to keep the basic narrative uninterrupted, a description of the RSFQ circuit layout, a brief pre-history of the digital single-flux-quantum digital devices, and a discussion of prospects for the high-T_c superconductivity are included in the Appendixes.

II. ABC's OF THE RSFQ

A. Handling the SFQ Pulses

Let us repeat that in the RSFQ logic circuits the signals are passed in the form of very short pulses $V(t)$, nominally with the area expressed by (1). In order to fully appreciate this choice, consider again the most elementary circuit shown in Fig. 1(a), but now with an overdamped Josephson junction. Fig. 1(c) shows the dc I-V curve of the junction; in contrast to the underdamped case, the curve is single-valued. It implies that after a current pulse $I_{in}(t)$ the junction is self-reset again to its original superconducting state.

This is a truth, but not all the truth. Elementary calculations using the Josephson dynamics equations show (see, e.g., [11] ch. 5) that if the pulse $I_{in}(t)$ is short enough, there exists a broad range of its amplitude within which the pulse induces a quantized leap of the Josephson phase ϕ of the junction: $\Delta\phi = 2\pi$; see Fig. 1(d).

This fact can be readily understood starting from the well-known analogy between the Josephson junction and the pendulum. In this analogy, biasing of the junction with the dc current $I_b \gtrsim I_c$ corresponds to applying a nearly critical torque to the pendulum, driving it to a position close to the critical angle $\phi_c = \pi/2$. The short input current pulse is equivalent to a kick that drives the pendulum beyond ϕ_c. If the pendulum is overdamped, the kick results in just one 2π-rotation of the pendulum with its return to the subcritical state.

According to the fundamental phase-to-voltage relation

$$\frac{d\phi}{dt} = \frac{2e}{\hbar}V(t) \qquad (2)$$

such a ''2π-leap'' of ϕ (in the literature, one can also find the term ''Josephson phase slip'' for essentially the same process) corresponds to the SFQ voltage pulse (1) across the junction. Duration of the pulse is close to the characteristic time unit

$$\tau_0 = \pi\omega_c^{-1}, \quad \omega_c = (\hbar/2e)V_c, \quad V_c = I_c R_{ef}$$
$$R_{ef}^{-1} = R_n^{-1} + R_s^{-1} \qquad (3)$$

where R_n is the effective normal resistance of the junction at voltage of the order of V_c, and R_s is the active impedance of the electrodynamic environment as seen by the junction. Table I

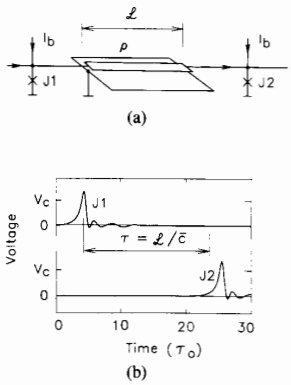

Fig. 2. Two overdamped junctions connected by a matched microstrip line. (a) Equivalent circuit and (b) simulation of the circuit dynamics (for $I_{c1} = I_{c2} = I_c$, $R_{ef1} = R_{ef2} = R$, $\rho/R = 1$, $I_b/I_c = 0.8$).

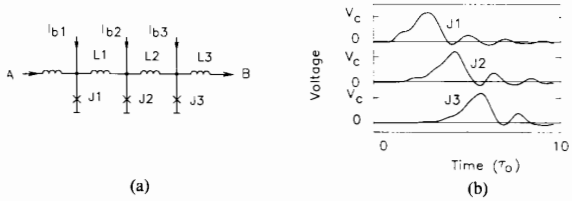

Fig. 3. SFQ transmission/amplification line. (a) Equivalent circuit and (b) results of the dynamics simulation (for $I_{bi} = 0.75I_{ci}$, $L_iI_{ci} = 0.5\Phi_o$).

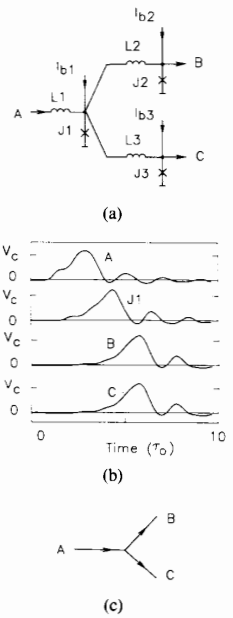

Fig. 4. The SFQ pulse splitter. (a) equivalent circuit. (b) Results of the dynamics simulation (for $I_{c2} = I_{c3} = I_c$, $I_{c1} = 1.4I_c$, $I_{bi} = 0.75I_{ci}$, $L_2 = L_3 = 0.6\Phi_o/I_c$), and (c) notation [30].

shows that for decent present-day fabrication technologies ($a \sim 1$–2 μm) the unit is close to one picosecond, so that the pulse amplitude $V_{max} \cong 2V_c$ is of the order of 1 mV. (The energy $\Delta E \cong I_c\Phi_0$ dissipated during the pulse is independent of a provided that I_c is fixed by thermal fluctuation stability considerations; see Appendix 3. The energy is of the order of 2×10^{-19} J for the value $I_c = 100$ μA typical for the helium-temperature operation.)

Calculations [31] show that if the dc bias current I_b is close enough to the critical value I_c, this SFQ pulse can be triggered, in particular, by a similar pulse, with either the nominal or a somewhat smaller amplitude. It means that the circuit shown in Fig 1(a) can *reproduce* the SFQ pulses, bringing their area to the nominal value (1), i.e., providing *voltage gain* if necessary. On the other hand, if the input pulse is too weak (say, presents a "noise" due to parasitic crosstalk between the signal transfer lines) it is not reproduced by the circuit, so that it also serves as a noise discriminator.

Two important remarks should be made here. First, the load (R_l in Fig. 1(a)) should not necessarily be an ohmic resistor; more typically, another similar junction serves as a load in the RSFQ circuits (Fig. 2(a)). Second, these junctions need not necessarily be close to each other; they can be connected by a long ($\mathcal{L} \gg \bar{c}\tau_0$) superconducting microstrip line of an appropriate wave impedance $\rho \simeq R_l$ (Fig. 2(b)).

Fig. 3(a) shows another key circuit comprising several Josephson junctions connected in parallel by superconducting strips of a relatively low inductance $L \sim \Phi_0/I_c$, and dc-current-biased to their precritical state ($I_b < I_c$). Let the 2π-leap of the Josephson phase in the left junction J1 of this array be induced by the input pulse. Calculations show that the resulting SFQ pulse developed across J1 will necessarily trigger the 2π-leap in J2, and this process will continue until the pulse is reproduced at the right edge of the array (Fig. 3(b)).

In order to develop a convenient way to look at this process let us recall that according to the Faraday induction law $\Phi = V$, the development of the SFQ pulse (1) across a two-terminal circuit element can always be considered as a result (or the reason) of it being crossed by a bunch of magnetic field lines carrying exactly one magnetic flux quantum $\Phi_0 = h/2e \cong 2.07 \times 10^{-15}$ Wb. If such a single flux quantum enters the array across an edge junction, it has no other choice than to leave it by crossing all the junctions in turn (flux crossing of the superconducting leads connecting the junctions is forbidden by the Meissner effect, and small inductances L of the leads make it impossible for the flux to be trapped in the loops of the array). Below, the reader will meet other examples where this "magnetic" language is more natural than that of the voltage pulses.

Coming back to the circuit shown in Fig. 3(a), we have seen that it is capable of *transferring* the SFQ pulses with a small time delay of order of τ_0 (Fig. 3(b)). The circuit can also *amplify* the pulses (more exactly, provide their *current and power gain*). For that, critical currents of the junctions (and the corresponding dc bias currents) should grow in the direction of the pulse propagation ($I_{c1} < I_{c2} < \cdots$), with the proportional decrease of the inductances ($L1 > L2 > \cdots$). For example, an exponential growth of I_c by a factor of $\sqrt{2}$ per stage provides quite a high current gain together with large ($\pm 30\%$) parameter margins; practically two or three junctions are sufficient.

An evident generalization of the circuit (Fig. 4(a)) provides *splitting* of the pulse, i.e., reproduction of the input pulse A at each of its two outputs B and C, without a decrease of the pulse voltage amplitude.

These simplest circuits are, however, not always practical: in

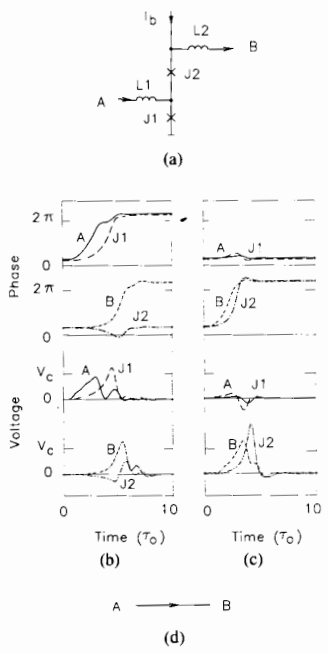

Fig. 5. The simplest RSFQ buffer stage. (a) Equivalent circuit and (b), (c) its dynamics (for $I_{c1} = 1.4I_{c2}$, $I_b = 0.7I_{c2}$, and (d) notation [25].

particular, inputs and outputs in Figs. 1–3 are reciprocal, so that the circuits cannot be used for isolation. Nevertheless, a slight modification yields a decent buffer stage (Fig. 5(a)). In this circuit, critical current of the junction J2 is somewhat smaller than that of the junction J1. Now, if the initial pulse arrives from the circuit input A, it is applied to J1 alone, and induces the 2π-leap of the Josephson phase in J1, leaving the phase across J2 virtually undisturbed (Fig. 5(b)). As a consequence, the SFQ pulse is reproduced and passed to the output terminal B.

On the contrary, if a pulse arrives from the latter terminal, it induces a current pulse in both J1 and J2. As $I_{c2} < I_{c1}$, the junction J2 reaches its resistive state earlier, and performs the 2π-leap of its phase, preventing J1 from the similar leap. Hence voltage across J1 remains close to zero, which means that the SFQ pulse does not reach the input terminal A (Fig. 5(c)).

Fig. 6 shows a generalization of this circuit—the "confluence buffer" that permits channeling of the SFQ pulses passing from both its inputs A and B to the single output C. Here, the auxiliary junctions J3 and J4 protect the inputs from penetration of the SFQ pulse from output C or another input. A negative feature of this simple circuit is that it can provide only one output pulse if the input pulses arrive too close in time.

B. SFQ Flip-Flops: Storing the Single Flux Quanta

Fig. 7 shows another key component of virtually all RSFQ circuits. It is essentially the celebrated superconducting quantum interferometer (sometimes called the dc SQUID) using two similar Josephson junctions ($I_{c3} \approx I_{c4} \approx I_c$). If the inductance L of the interferometer is chosen to make its basic parameter

$$\beta_l = 2\pi \frac{LI_c}{\Phi_0} \tag{4}$$

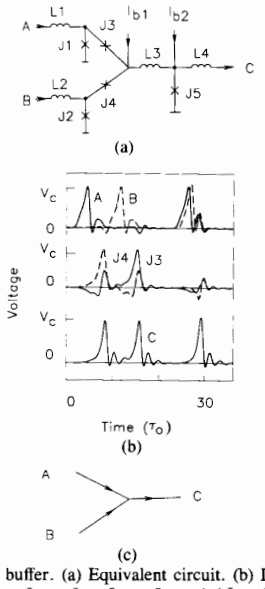

Fig. 6. Confluence buffer. (a) Equivalent circuit. (b) Its dynamics simulation (for $I_{c3} = I_{c4} = I_{c5} = I_c$, $I_{c1} = I_{c2} = 1.4I_c$, $I_{b1} = 1.4I_c$, $I_{b2} = 0.7I_c$, $L_3 = 0.5\phi_o/I_c$), and (c) notation.

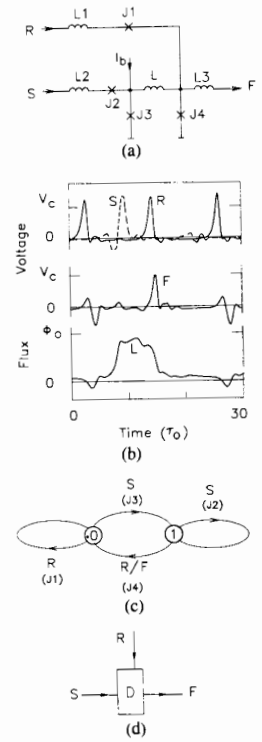

Fig. 7. SFQ RS flip-flop (used typically as the DRO register cell). (a) The equivalent circuit. (b) Dynamics (for $I_{c1} = I_{c2} = I_c$, $I_{c3} = I_{c4} = 1.41I_c$, $I_b = I_c$, $L = 1.25\Phi_o/I_c$)). (c) The Moore (state-transition) diagram. (d) Notation of the circuit [25]. Josephson junctions that perform the 2π-leaps of their phase during particular state transitions are indicated in parentheses in the Moore diagram. Point denotes the initial state which is established after turning on the dc bias.

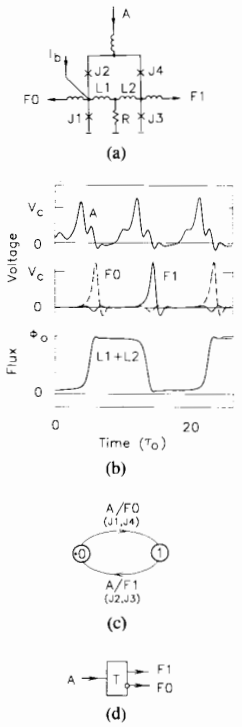

Fig. 8. SFQ T flip-flop. (a) Equivalent circuit. (b) Dynamics (for parameters similar to those in Fig. 7). (c) The Moore diagram. (d) Notation [27].

close to 10, and the dc bias current I_b is close to 0.8 I_c, the circuit has two symmetric stable stationary states that differ by the direction of the persistent current $I_p \approx \pm \Phi_0/2L$ circulating in the loop. In the •"magnetic" language, one of these states corresponds to an additional single flux quantum trapped in the superconducting loop of the interferometer. Let us suppose that the persistent current is circulating counterclockwise (binary "0"), so that it sums up with I_b in J3: $I_3 = I_b/2 + I_p \sim I_c$. If now the SFQ pulse (possibly, with a somewhat decreased amplitude) arrives at the input S, it induces the 2π-leap in J3, but not in J2, which carried a lower dc current. As a result of the leap, the cell is switched to its opposite "1" state with the clockwise circulation of the persistent current. It is evident that now the reset ("1"→"0" switching) can be triggered by the SFQ pulse arriving at the R terminal. Simultaneously, an SFQ pulse $V(t)$ is developed across J4, which can serve as an output signal F. The auxiliary junctions J1 and J2 defend the SFQ pulse sources from the back reaction of the interferometer in the case of a "wrong" signal, for example, of the S pulse arriving during the "1" state. In this case, junction J2 (rather than J3) switches; in the "magnetic" language, the incoming single flux quantum "falls out" of the circuit through J2 if the interferometer loop is unable to accept it.

One can see that for the SFQ pulses the circuit works exactly as a standard RS flip-flop (trigger). The SFQ pulses can be trapped by this circuit, so that the information about their arrival there can be conveniently stored there, and released when necessary in the similar physical form.

Fig. 8 shows the SFQ analog of the *T flip-flop* (i.e., a single bit stage of the *binary counter*). This circuit is fed by the input

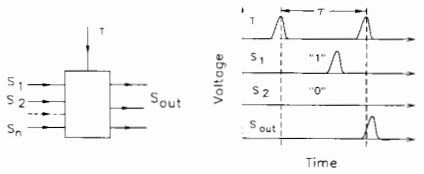

Fig. 9. An elementary cell of the RSFQ circuits. (a) The general scheme. (b) Signal consequence.

pulses from its single input A. Each pulse is split (c.f., Fig. 4(a)) and injected to both arms of the interferometer, so that it always triggers the circuit switching to the opposite state. An important auxiliary component of the circuit is the resistor R between the middle point of the interferometer inductance and the ground. It somewhat prolongs the switching process and substantially widens the parameter margins. Experimentally measured margins for the dc bias current I_b were as wide as ±30% [26] for this circuit, in a good agreement with numerical simulations.

C. RSFQ Basic Convention: Presentation of Bits

The above physical background enables one to describe the general idea of storing, passing, and processing the binary information in the RSFQ circuitry. Any RSFQ circuit consists of *elementary (logic/memory) cells*, operating as Fig. 9 shows. The cell is fed by the SFQ pulses that can arrive from one or several *signal lines*, $S_1, \cdots, S_n$, and the *clock (timing) line* T. (For the beginning, it is easier to think about the T pulses as arriving periodically in time, although we will see later that their periodicity is an exception rather than a rule in practical RSFQ circuits.)

Generally, each cell can have two or more stable states (cf., the flip-flop states described above) and hence presents a finite-state machine from the point of view of general computer science [32]. Each clock pulse marks a boundary between two adjacent *clock periods* by setting the cell into its "0" state. During the new period, an SFQ pulse can arrive (or not arrive) at each of the cell inputs S_i (Fig. 9(b)), changing the cell state. This is the right moment for formulation of the *RSFQ Basic Convention*:

Arrival of the SFQ pulse to a terminal S_i during the current clock period has a meaning of the binary "1" value of the signal S_i, while absence of the pulse during this period is understood as the binary "0" value of this signal.

Note that the convention does not require an exact *time coincidence* of the SFQ pulses (it would be impractical because of their picosecond duration). Moreover, neither a certain *time sequence* of the various input signals is needed; the only requirement of the Basic Convention is that each pulse denoting the binary "1" arrives *some time* during the clock period. Each pulse either changes or does not change the internal state of the cell, but *it does not produce any immediate reaction at its output terminal(s) S_{out}*. Only the clock pulse T is allowed to develop the output pulse(s) S_{out} corresponding to the internal state of the cell, predetermined by the input signal pulses which arrived during this period. The same clock pulse terminates the clock period by resetting the cell. Thus an elementary cell of the RSFQ family is equivalent to a usual asynchronous logic circuit coupled with a register (flip-flop) storing its output bit(s) until the end of the clock period.

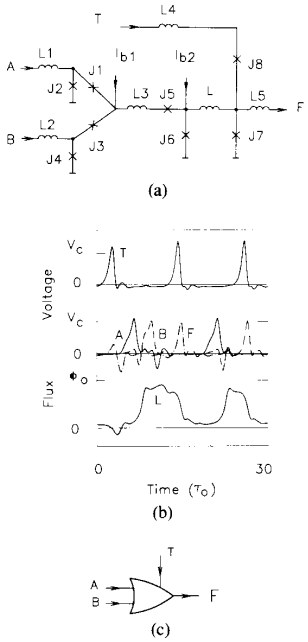

Fig. 10. OR cell. (a) The equivalent circuit. (b) Dynamics for $\{A = 1, B = 1\}$ and $\{A = 1, B = 0\}$. (c) Notation [25].

III. Basic Elementary Cells

A. OR Cell

In order to understand why the combined logic/memory circuits are used as the elementary cells of the RSFQ family, let us have a look at how simply these cells can be composed from the basic components considered in Section II-A and -B.

For example, in order to get the 2-input *OR cell* (Fig. 10(a)) it is enough to unite the confluence buffer (Fig. 6(a)) with the *RS* flip-flop (Fig. 7(a)). When the SFQ pulse arrives at one of the signal inputs (A, B) it is reproduced (normalized) by the buffer stage and then is fed into the input of the flip-flop, either inducing its "0"→"1" switching (if it is the first signal pulse during the given clock period) or having no effect on its internal state. (If the switching has been already triggered by the preceding signal pulse, the signal pulse induces the 2π-leap of the phase in the junction J5.) Even if the signal pulses (occasionally) coincide in time, their final effect on the circuit is similar to that of a single pulse. Note also that no SFQ pulse appears at the circuit output during the clock period; the output can appear (if at least one signal has arrived during the period) only as a result of the circuit being reset by the clock pulse arriving to the T input and thus terminating the clock period.

One can be readily convinced that within the RSFQ Basic Convention, the circuit does perform the "timed" OR function, with the output delayed until the end of the clock period. It is also useful now to have one more glance of Fig. 9 and the accompanying description of operation of the arbitrary RSFQ cell. The reader will probably agree that this type of operation is not something artificial but rather the most natural utilization of the unique dynamics of the Josephson junction circuits.

B. DRO and NDRO/DRO Register Cells

It is evident that the *RS* flip-flop (Fig. 7) itself presents a latch, i.e., a single-bit cell of a "*D register*" with destructive read-out (DRO), if its S input is fed with the signal pulses, while the R input is fed with the clock pulses. A ready modification (Fig. 11) turns this circuit into a cell of an "*N register*" permitting the nondestructive read-out (NDRO) as well.

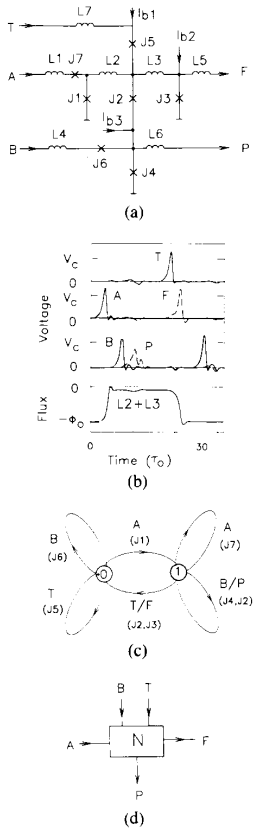

Fig. 11. NDRO/DRO register cell. (a) The equivalent circuit. (b) Dynamics. (c) Moore diagram. (d) Notation of the cell [29]. The left part of Fig. 11(b) illustrates the WRITE operation, while its middle part, the NDRO operation, and right part, the DRO operation of the cell.

The main new feature here is the addition of a new pair of Josephson junctions J2, J4 connected in series to a middle point of the two-junction interferometer (J1, J3, L2, L3). Critical current of the additional junction J2 is relatively low, so that the addition does not influence statics and dynamics of the interferometer qualitatively. This is why the cell operates as the simple DRO register, when its inputs A and T are fed by the signal and clock SFQ pulses, respectively (in this mode the output bit appears at the terminal F).

The effect of the cell state on the junction pair J2, J4 is, on the contrary, quite considerable. In the "1" state, with its clockwise circulation of the persistent current, the net phase drop across each junction of the pair is close to $\pi/2$, so that junction J4 is in a precritical state ($\phi_i \approx \pi/2$, $I_i \approx I_C$). In this case, arrival of an SFQ pulse from the terminal B induces two successive 2π-leaps (first in J4 and then J2 junctions), and the SFQ pulse is reproduced at the NDRO output terminal P. It is important that this switching does not change the internal state of the cell (Fig. 11(b)). In the opposite "0" state, the junctions J2, J4 are far from their critical state, and the NDRO-initiating pulse B induces the 2π-leap in the junction J6 rather than in any of J2, J4.

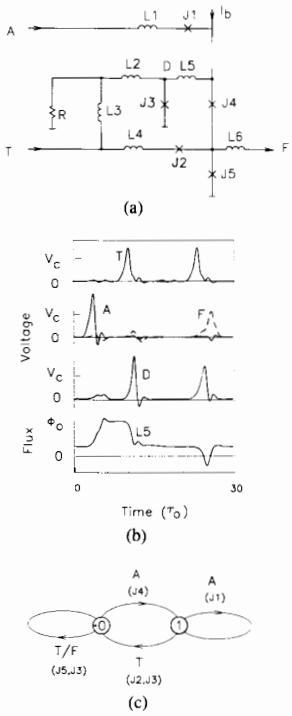

Fig. 12. RSFQ inverter. (a) The equivalent circuit. (b) Dynamics for $A = 1$ and $A = 0$. (c) Moore diagram.

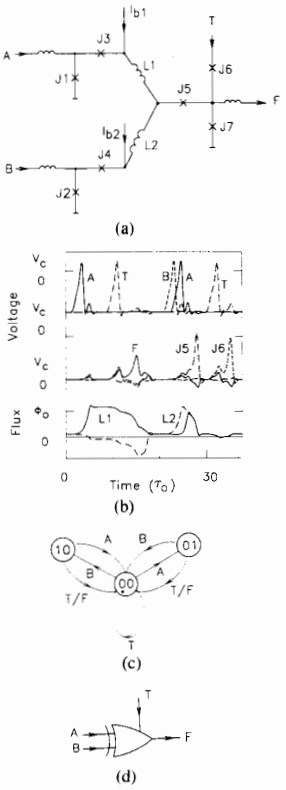

Fig. 13. Exclusive OR cell. (a) The equivalent circuit. (b) Dynamics for $\{A = 1, B = 1\}$ and $\{A = 1, B = 0\}$. (c) The Moore diagram. (d) Notation [30].

As a result, the zero output P again mirrors the contents of the register.

Note that if the pulse B is considered as a signal rather than the NDRO clock, the same circuit performs the asynchronous single-bit multiplication (in other words, the AND function) provided that the B pulse arrives later than A.

C. Inverter

Fig. 12 shows another modification of the basic flip-flop, which leads to a cell performing the signal *inversion* (*NOT function*), one of the most difficult tasks in any Josephson junction digital technology (cf., [4], [6], and [22]). Here, the additional Josephson junction J5 is inserted in series into the main quantizing loop (J3, J4, J5, L5) of the cell. Critical current of this additional junction is relatively large, so that the SFQ signal pulse A induces a 2π-leap in J4 rather than in J5. As a consequence, the resulting "0"→"1" switching of the cell produces no considerable signal across the output terminal F. The clock pulse T induces the 2π-leap in J2 (but not in J5, because of its larger I_c), and there is no output pulse again. However, the same clock pulse, after a small time delay by the circuit L3, R, L2, arrives at the terminal B and resets the cell to its "0" state by inducing the 2π-leap in J3.

On the other hand, if there were no signal pulse during the operation period, and the cell remains in its "0" state until the clock pulse T, the latter pulse finds the persistent current flowing counterclockwise, and the junction J5, in its subcritical state. Hence the 2π-leap is induced in this junction rather than J2, and an SFQ pulse is formed at the output terminal F.

D. XOR Cell

One more fruitful way to modify the basic SFQ flip-flop is to split one of its arms. In particular, such a splitting allows one to perform the two-input *exclusive* OR (XOR) function (Fig. 13). Due to the splitting of the basic interferometer, the cell can be considered as consisting of two quantizing loops (J1, J3, L1, J5, J7, and J2, J4, L2, J5, J7). As a consequence, the cell has three stable static states. One of them ("00") can be interpreted as that without trapped flux quanta, and two others ("01" and "10") as those with a single flux quantum trapped in the loops containing junction J1 or J2, respectively. (Simultaneous trapping of two flux quanta, i.e., the "11" state, is unstable due to the interaction of the cells via the common junction J5.) Dynamics of the cell are very similar to that of the elementary flip-flop (see Fig. 13(b) and (c)).

E. OR–AND Cell

We have seen that the cell shown in Fig. 11(a) can be used as the AND cell only under certain conditions. In order to get rid of this limitation, another AND cell would be quite useful. As an exception, this circuit does not require its own quantizing interferometer but can use those of the input cells, so that it is convenient to combine those to form one circuit performing a more general function.

Fig. 14(a) shows an example [34] of such a combined cell that performs the OR–AND *function*. Here the elements J5, J6, L1, L2, J7 can be considered as forming the AND circuit

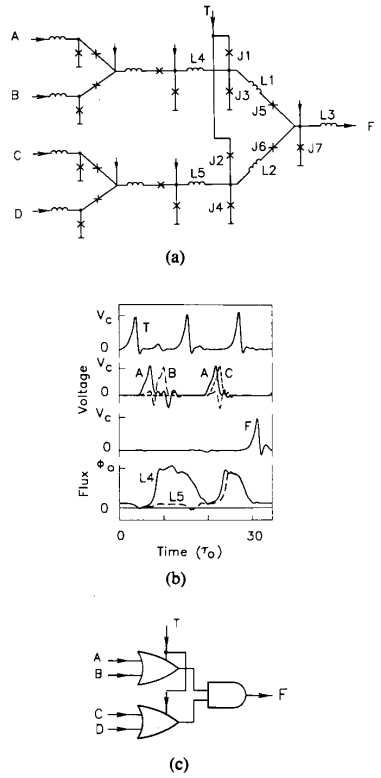

Fig. 14. Single-bit cell performing the generalized function $F = (A + B) \cdot (C + D)$. (a) Equivalent circuit. (b) Dynamics for $\{A = B = 1, C = D = 0\}$ and $\{A = C = 1, B = D = 0\}$. (c) Notation [34].

(cf., Fig. 6(a)), and the remainder as a couple of OR cells similar to that shown in Fig. 10(a). If both these OR cells are in their "0" state by the end of the clock period (which is possible only if $A = B = C = D = 0$), the clock pulse T switches junctions J1 and J2, with no appreciable effect on the output F. If *one* of the OR cells (say, that with junction J3) is in its "1" state, then J3 (rather than J1) is switched by T, so that the SFQ pulse is applied to junctions J5 and J7 connected in series. The former of these junctions has a smaller critical current than the latter one, so that J5 is switched, and there is no output pulse again. The only case when J7 switches and produces the SFQ pulse at the output F is when *both* OR cells are in their "1" state, so that *both* J3 and J4 are switched simultaneously by the clock pulse T. (In this case the pulse currents, injected into J7 through L1 and L2, sum up and exceed the critical current of this junction.)

Note that in contrast to other RSFQ cells, an exact time coincidence of the current pulses in L1 and L2 is essential in this circuit. However, this does *not* violate the RSFQ Basic Convention because these pulses are confined *inside* the cell; the input pulses A, B, C, D are free of this requirement. Numerical simulations show that the necessary coincidence is achieved inside a wide parameter window (the critical current margins can be in excess of $\pm 30\%$).

It is straightforward to modify this circuit by changing either one OR cell or both of them for cells performing other functions F_1 and F_2; in this case the combined cell will perform the function $F_1 \cdot F_2$. As the simplest extreme, a "bare" AND cell is

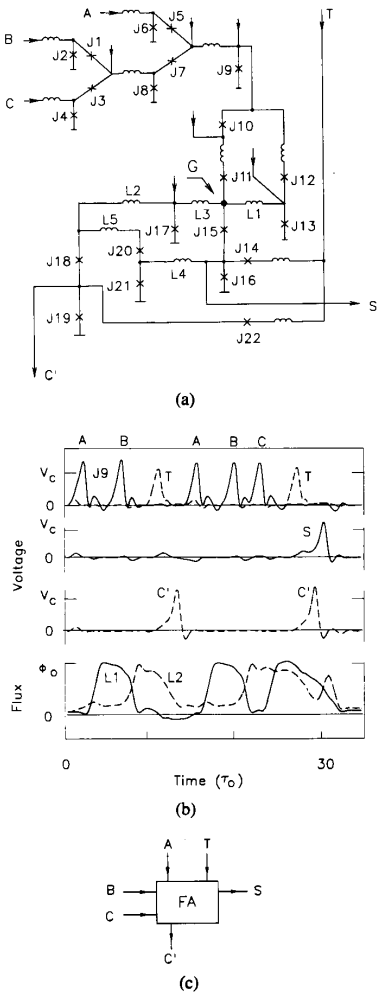

Fig. 15. Single-bit full adder. (a) The equivalent circuit. (b) Dynamics for $\{A = B = 1, C = 0\}$ and $\{A = B = C = 1\}$. (c) Notation [25].

readily possible (with the DRO register cells in the both inputs), but too hardware-consuming.[1]

F. Single-Bit Full Adder

The last elementary circuit we will need for our further discussion is the single-bit *full adder* (FA). Generally speaking, it can be readily composed in the usual way (see, e.g., [74]) from two XOR cells, two AND cells and an OR cell. Fig. 15(a)

[1] There is another example of modification of an element with restrictions on mutual time shifts between input pulses in order to meet the full RSFQ convention. The asynchronous confluence buffer, as mentioned above, can generate one or two output pulses depending on the time shift between its two input pulses, thus violating the RSFQ basic convention. Moreover, there is a nonvanishing transition range of these shifts where confluence buffer operates improperly. To eliminate time shifts of this range one can use an element that consists of two clocked flip-flops followed by the confluence buffer. Similar to the OR-AND cell, the same clock pulse is used for reading out both the flip-flops, ensuring the fixed delay between output pulses and hence the correct operation of the confluence buffer. This does not mean that one has to add new flip-flops to all confluence buffers. Usually it is sufficient to consider logic cells followed by the confluence buffer as a single element.

TABLE II
PARAMETERS OF THE BASIC ELEMENTARY CELLS AND SOME AUXILIARY CIRCUITS OF THE RSFQ FAMILY

Circuit	Time delay, δ/τ_O	Number of JJ	Area, A/a^2	Margins, ± %
I. Elementary cells				
DRO register	2	4	500	30
OR cell	3	9	900	30
AND cell	1	3	400	30
NDRO/DRO register	2	6	700	20
Inverter	3	5	580	25
XOR cell	3	7	800	20
1-bit full adder	8	22	2500	[b]
1-bit stage of the serial memory Register	1	2	250	30
II. Auxiliary circuits				
Buffer stage	1	2	200	50
Split buffer	1	1	210	50
Confluence buffer	2	5	570	30
Coincidence junction	2	3	50	35
DC/SFQ converter	2	2	200	40
SFQ/dc converter	[a]	6	680	30
1-bit multiplexer	1	10	1100	[b]
1-bit demultiplexer	1	14	1300	[b]

[a] Depends substantially on the dc load.
[b] To be calculated.

shows the result of our first attempt [25] to develop a simpler adder, while Fig. 15(b) shows results of numerical simulation of its operation for two and three input pulses.

The cell has two quantizing loops (J13, L1, J15, J16) and (J17, L2, J18, J19), with two stable states each. The former interferometer is fed by the signal pulses A, B, and C through the confluence buffers, and operates as a T flip-flop (cf., Fig. 8). As a result, a correct sum bit pulse S is formed across junction J16 under the action of the clock pulse T (Fig. 15(b)).

It is easy to check that a correct carry bit pulse is being formed in the point G. One cannot use it, however, because the sum bit pulse also penetrates there. The remaining part of the adder serves to cut off this parasitic sum signal. If $S = 0$ and $C' = 1$, the genuine carry bit pulse switches the persistent current in the loop L2 to flow counterclockwise, and is thus correctly read out to the output C' by the clock pulse T. On the contrary, if $S = 1$ and $C' = 1$, the clock signal, after some delay, also arrives at the opposite arm of the interferometer through the buffer circuit J4, J20, L5. By switching the junction J19 this delayed pulse resets the interferometer to its proper state (Fig. 15(b)). As a reward for these complications, the correct carry bit pulse is formed at the terminal C' with a considerable delay after the clock pulse T. We will see that this delay enables one to use this cell as a very simple serial adder.

We are not, however, quite happy with this circuit. Firstly, it does not tolerate an occasional coincidence of the input pulses (cf., Fig. 6 and its discussion). Secondly, its parameter margins are rather narrow. A better design is in progress presently.

G. Parameters of the Elementary Cells

The very concept of the elementary cells (see Fig. 9 and its discussion) supposes that the time delay between an input and output of the cell cannot exceed the clock period τ. For a particular cell there is of course a minimum value δ of the period τ for which the cell operates correctly. Table II shows this value for the elementary cells considered above; δ is expressed in the natural units τ_0; for the standard "niobium" technology this unit is directly determined by the linear size a of the junction (which practically coincides with minimum feature size); see Table I.

Table II also gives an estimate of the cell area A in units of a^2 and shows the total number of the Josephson junctions in the cell (these numbers can serve as a measure of the cell complexity).

Several auxiliary circuits (both considered above and to be discussed in Sec. V) are also listed in Table II. For them, δ should be understood as an explicit time delay between the input and output SFQ pulses.

The same table shows parameter margins. They were calculated using the operational range option of the PSCAN program [34] as a maximum relative variation of the junction area, which does not lead to misfunctioning of the circuit. (Other possible definitions of the margins lead to nearly similar values.) One can see that the RSFQ circuit margins are not less than those of the modern latching gates (see, e.g., [22]).

TABLE III
ESTIMATES OF BASIC PARAMETERS OF 32 × 32-BIT FIXED-POINT MULTIPLIERS BASED ON VARIOUS DIGITAL CIRCUIT TECHNOLOGIES [29]

Circuit type; fabrication technology (design rules)	Integration scale (Josephson/p–n junctions per chip)	Productivity (billion operations per second)	Time delay (ns)
Parallel pipelined; Si-MOS (1.0 μm)	200 000	0.2	150
Parallel; GaAs (0.5 μm)	100 000	0.15	6
Parallel; JJ latching (2.5 μm)	70 000	0.5	2
Serial; JJ RSFQ (2.5 μm)	1 500	0.5	2
Parallel-pipelined; JJ RSFQ (2.5 μm)	40 000	30	2

IV. SOME LOGIC AND ARITHMETIC BLOCKS

A. The Simplest Serial Blocks

Now it is straightforward to use the single-bit cells described in Sec. III for building logic and arithmetic blocks performing either serial or parallel processing of multibit data, so that we will consider only a few examples of these. (For the sake of convenience we will leave discussion of the key problem of timing until the next section; here we will imagine that the necessary clock pulses arrive in due time from the environment of the block.)

First of all, some logic/arithmetic operations with multibit numbers can be performed using just *one* single-bit cell. For example, consider an operation where any bit of the result is a function of the corresponding bits of the input numbers (say, the n-bit OR function). One can perform this operation *in series* by consequently feeding the input bits into the proper single-bit cell and picking up one single bit of the result F after each clock pulse (Fig. 16(a)).

The next example is the *serial addition* of two multibit

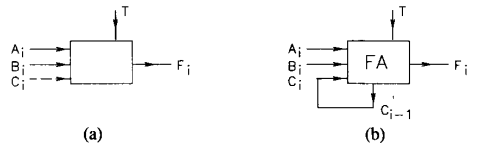

Fig. 16. The simplest serial blocks for (a) elementary logic operations, and (b) summation of the multibit numbers.

numbers A and B, where each single-bit addition requires not only current signal bits A_i and B_i, but also the carry bit $C_i = C'_{i-1}$ produced during the preceding clock period. This problem is, however, readily solved by the circuit shown in Fig. 16(b). (One does not need to insert any time delay into the carry bit line, because the C'_{i-1} pulse is generated with some delay after the clock pulse T, i.e., arrives to the input terminal C safely after the beginning of the next clock period.)

B. Serial ALU

The same approach can be applied to the design of more complex serial devices, in particular, *arithmetic/logic* units (ALU). Most instructions of a typical ALU can be fulfilled in a serial way, starting from the least significant bits. (An important exception are rotate-type instructions; in RSFQ circuits they can be readily fulfilled using ring registers; see Section V.)

This is why the serial ALU can be designed in a way similar to the serial adder (Fig. 16(b)) with the exception that the single-bit cell should perform a function controlled by the instruction code. Such a cell can be composed of the elementary cells discussed in Sec. III (see, e.g., [22]), supplemented by switching (multiplexer/demultiplexer) circuits. Such switching can be performed by a combination of the cells N (Fig. 11) and split/confluence buffers (Figs. 4 and 6). The special multiplexer and demultiplexer circuits, shown in Fig. 17, are, however, more convenient. Each of these very similar circuits is controlled by S/R pulses of the instruction code, which can switch the state of the symmetric interferometer J7, J3, L, J4, J8 and thus establish what arm of it (right or left) becomes transparent for the signal SFQ pulses. In the multiplexer (Fig. 17(a)) the signal pulses A and B are independent, and are channeled to the general output F through the confluence buffer J11–J14. In the demultiplexer (Fig. 17(c)) the single input pulse A is passed to one of the outputs $F1$, $F2$.

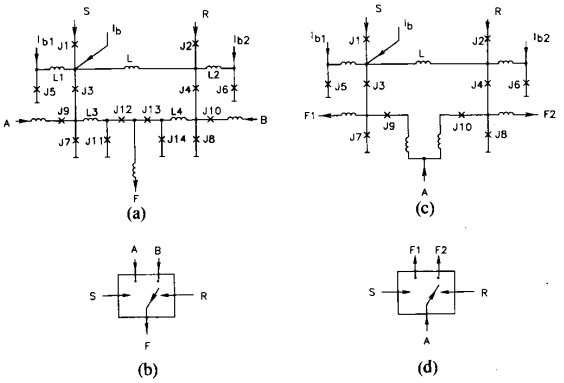

Fig. 17. RSFQ pulse switches. (a) Multiplexer. (b) Demultiplexer. (c), (d) Their functional schemes [34].

C. Serial Multiplier

Multiplication of n-bit numbers requires more complex circuits with the number of the elementary cells scaling either as n, or even as n^2. Fig. 18(a) shows a possible structure of the block *SM* performing the serial multiplication of numbers A and B. The block uses three types of the single-bit elementary cells: DRO sells D (i.e., RS flip-flops, Fig. 7), DRO/NDRO sells N (Fig. 11), and full adders FA (Fig. 15) operating as the serial adders (cf., Fig. 16(b)). Operation of the block is controlled by two sequences ("trains") of the clock pulses, T_A and T_B (Fig. 18(b)).

The operation is started by a train of n clock pulses T_B arriving to all cells N. The train induces sequential loading of the B bits into the shift register formed by these cells. Then the train T_A starts, which induces a similar loading of the bits of A into the shift register formed by the D cells. The latter train induces also a simultaneous backward motion of the bits along the string of the full adders FA.

One can be readily convinced that in the end of each operation

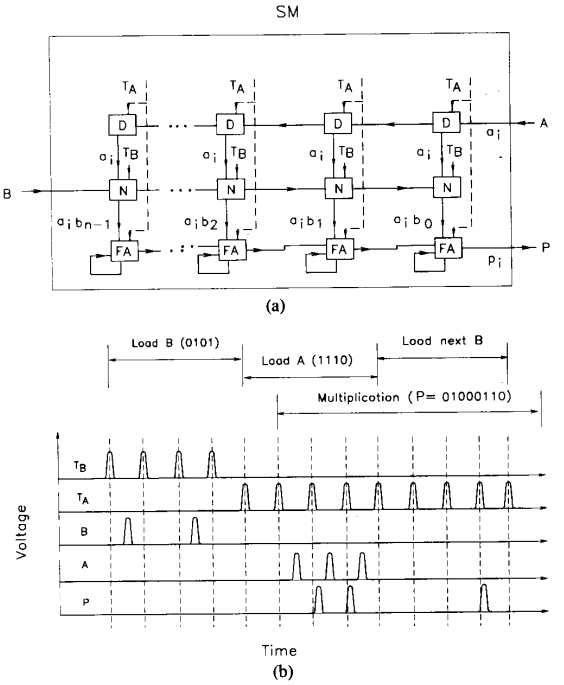

Fig. 18. Serial RSFQ multiplier. (a) The block circuit and (b) pulse consequence for B = "0101" and A = "1110" [28].

period terminated by a pulse T_A the block really produces the correct consequent bit of the $2n$-bit product $A \cdot B$ at its output terminal P. (In fact, all the partial single-bit multiplications are performed by the N cells, while the serial adders FA merely sum up all the partial products.)

Note that the whole multiplication takes $2n$ clock periods (loading of the next B can be fulfilled during last n periods of the previous multiplication cycle; see Fig. 18(b)). A numerical estimate of the time necessary for the operation will be presented below (Table III).

D. Serial Divider

Fig. 19(b) shows an arithmetic block D_j for serial calculation of the n-bit reciprocal $F = 1/M$ $(1/2 < M < 1)$ via $k =$

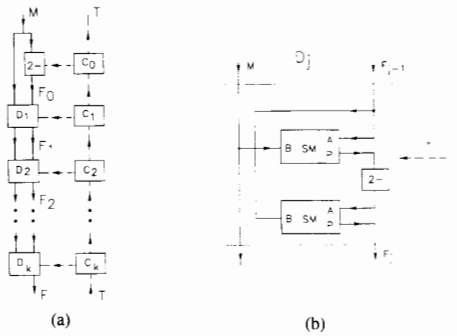

Fig. 19. Serial divider. (a) The block circuit. (b) Structure of the block D_j [28].

$\log_2 n$ iterations using the well-known recipe:

$$F_j = F_{j-1}(2 - M \cdot F_{j-1}) \tag{5}$$

starting with $F_o = 2 - M$ (each iteration doubles the number of correct bits). The block consists of two serial multipliers *SM* (Fig. 16(a)) and a simple device "2-" calculating the difference between 2 and the input number. (The latter device consists of two single-bit cells, the inverter and the full adder.) The "pipeline" structure of the block allows the cycle time of one iteration to be somewhat less than that required for two multiplications.

The complete divider can be arranged in two different ways; the simplest one is to link the F_{j-1} and F_j terminals of a single D block by the shift register and to run it during $\log_2 n$ cycles, while the other one is to use a pipeline structure (Fig. 19(a)) composed of $\log_2 n$ blocks D_j with increasing bit lengths ($n_j \cong 2_j$). The total division time for these two cases is $\sim 2n \cdot \log_2 n$ and $4n$ clock periods, respectively.

E. Parallel Multiplier

Productivity of calculations can be increased drastically using parallel-pipeline single-bit units. Fig. 20 shows an example of such a device, a multiplier of two n-bit numbers A and B (in our example, $n = 4$). It presents a two-dimensional array (Fig. 20(a) of single-bit multiplication units M shown in Fig. 20(b). (Most of the units do not get a complete set of input signals and can be internally simplified accordingly; in Fig. 20(a) one can see two types of the simplified units, the half-adder H and the DRO register cells D.) Note that the unit M is a copy of a single column of the serial multiplier (Fig. 18(a)); the only difference is a way of connection of the units and their timing.

If the clock pulses are fed into the vertical columns of the structure consequently, from right to the left (for implementation of that, see the next section), the signal bit front is moving from left to the right, being processed simultaneously. If fed in parallel by all $2n$ bits of new operands (A, B) each clock period, this "pipeline" multiplier produces *all* $2n$ *bits* of the product $P = A \cdot B$ *during one period*, although a full processing of each specific pair of the operands takes $2n + 1$ clock periods.

F. Parallel–Serial Blocks

The above examples demonstrate that the serial blocks have the following common features: they consist of $N \times n$ elementary cells and produce M output bits during each clock period, where n is the bit number, and N and M are some integers independent of n and generally not much larger than unity. On the other hand, a parallel block requires $N \times n^2$ cells and produces $M \times n$ bits per period.

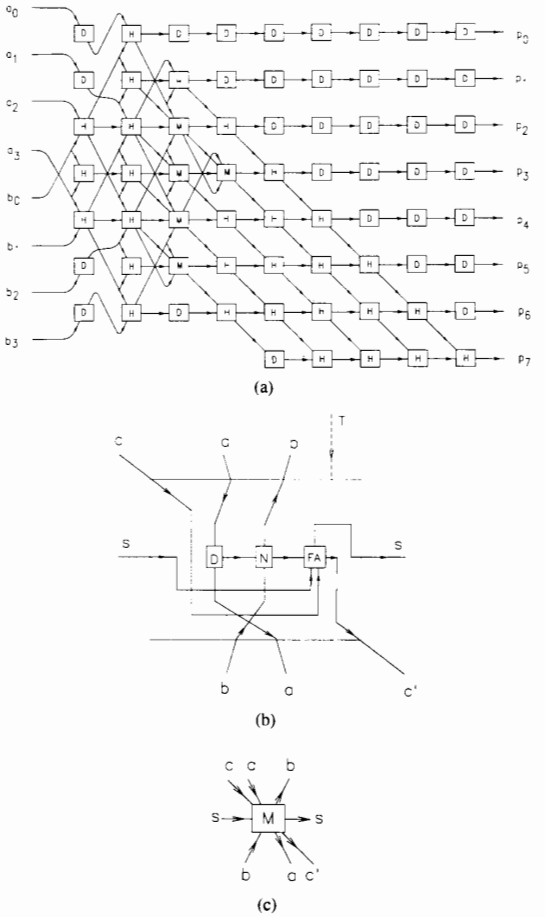

Fig. 20. Parallel RSFQ multiplier. (a) General structure. (b) That of its single cell. (c) Notation of the cell [28].

Nevertheless, one may need some blocks that escape from this classification. For example, one can increase the speed of the multiplier similar to that shown in Fig. 18(a) by using parallel m-bit multipliers shown in Fig. 20(a) (with $m < n$) instead of the single-bit multipliers. (Of course, the register cells D and full adders FA should be redesigned correspondingly.) Such a device would require a factor of m more junctions, but would operate $\sim m$ times faster.

V. Self-Timing

A. Elementary Cell Timing

Timing (synchronization) of the digital systems has always been a special computer science discipline (see, e.g., [10]). This discipline becomes of even larger importance for the systems being designed to operate at ultrahigh clock frequencies (say, beyond 100 GHz). The RSFQ logic is apparently the pioneer at this frontier, so that its timing deserves special attention.

The first fact to be fully appreciated is that *the external (global) synchronization of an LSI circuit at such frequencies is impractical*. In fact, it is hardly possible to debug the global synchronization circuit layout of minor imperfections

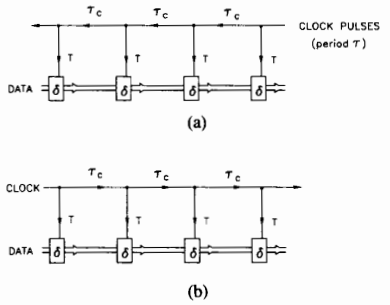

Fig. 21. The simplest clock distribution systems for (a) counterflow and (b) concurrent flow of the clock and signal waves in a one-dimensional RSFQ circuit. τ_c is the clock pulse delay, while δ is the cell delay.

producing pulse delays of the order of 1 ps. But at, say, 300 GHz clock frequency, such delays of the global clock signal are as a rule unpermissible! This is why the RSFQ-type superfast devices should rely on the *self-timing* of one or another type. The preferable type of timing is dependent on the size of the circuit fragment.

Let us start from smallest fragments, the elementary cells (Section III). Tables I and II show that for the present-day fabrication technologies ($a = 1$–2 μm), the delay δ of a typical cell is of the order of 5 ps, while its linear size is of the order of 30 μm. The SFQ pulse propagating along the typical superconducting microstrip line with velocity $\bar{c} \simeq c/\sqrt{\epsilon} \cong 10^{10}$ cm/s passes the latter distance in less than 1 ps, i.e., much faster than δ. This means that even considerable (say, fewer than 10%) changes or imperfections of the clock pulse propagation circuit layout cannot affect the circuit operation.

Hence most elementary cells can be controlled in a "lumped" way by clock pulses generated somewhere outside the cell.

B. Signal and Clock Pulse Waves

The last conclusion is valid also for some other RSFQ circuits, for example for the simplest arithmetic blocks, especially with a small wordlength (say, $n = 8$). For larger circuits, other approaches become necessary.

Let us consider them using a simple shift-register-type structure (Fig. 21) as an example. (Here and below the data transfer will be denoted by double lines and the clock, by single lines.) Before passing the data from the previous (sending) cell to the following (receiving) one, we should first complete the clock period of the receiver by resetting it with the clock pulse. The most evident way to ensure this consequence is to send the clock pulse train in the direction opposite to the desired signal propagation direction, with an appropriate time delay τ_c per gate (Fig. 21(a)). This "wave counterflow" timing scheme generally requires that

$$\tau, \tau_c > \delta \tag{6}$$

where τ is again the clock period, and δ is the maximum time delay of the cell. Under this condition, each clock pulse induces a shift of all contents of the register by *one* position.

In order to see whether another way of the simple timing is possible, consider an alternative scheme, shown in Fig. 21(b). This scheme can work correctly only if (6) is satisfied and the whole register is initially empty. In this case a single clock pulse will induce a motion of the *single* input bit along *whole* the register.

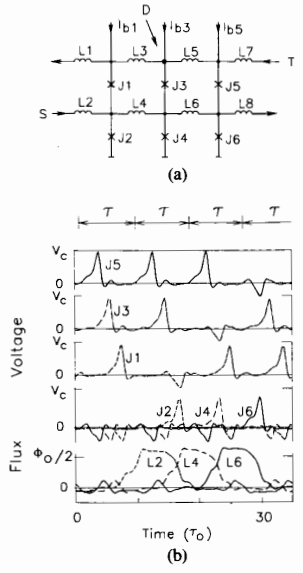

Fig. 22. A simple RSFQ shift register. (a) Equivalent circuit. (b) Dynamics for two cases described in the text [34].

Thus the simple timing circuits shown in Fig. 21 allow one to fulfill any of the basic tasks: either provide a one-step shift of contents of a register full with the data, or induce a rapid load of the data to an initially empty system. Their design should only satisfy the *local* condition (6) in order to ensure a correct operation of the system *as a whole*. Thus the natural intrinsic memory of the RSFQ cells enables one to avoid more complex two-phase timing schemes typical for the semiconductor circuits (see, e.g., [32]).

Note that Fig. 21 assumes that the data do not influence the clock pulse dynamics. In some specific circuits this rule can be somewhat violated, permitting very efficient designs. For example, Fig. 22(a) shows a shift register which can be used in very compact cash memories (only two Josephson junctions per bit) [33], [34]. The lower interferometers (J2, L4, J4, etc.) are quantizing and contain the data bits. The clock pulses T are propagating along nonquantizing loops of the upper row (cf., Fig. 3 and its discussion). If the pulse arrives to a junction column (say, J3, J4) which separates interferometers with similar states, it switches the upper junction (J3), because the persistent currents circulating in the interferometers cancel in the lower junction (J4) and it is far from its critical state.

On the other hand, if the states differ (say, L6 does not carry the persistent current denoting binary "0," while L4, the clockwise current denoting "1"), the persistent currents sum up in the lower junction (J4), driving it close to its critical state. In this case the clock pulse switches the lower junction rather the upper one. This event shifts the flux quantum (i.e., binary "1") from cell L4 to cell L6, and also somewhat influences the clock pulse dynamics, but does not change the very fact of the further propagation of the clock pulse (because switching of either J3 or J4 produces the SFQ pulse $V(t)$ in the point D). One can check that *all* "1"–"0" and "0"–"1" boundaries, and hence the whole the data string, will be shifted to the right after propagation of the single clock pulse along all the register, in accordance with the general "counterflow" scheme (Fig. 21(a)). The same circuit can also operate in the load mode (Fig. 21(b)).

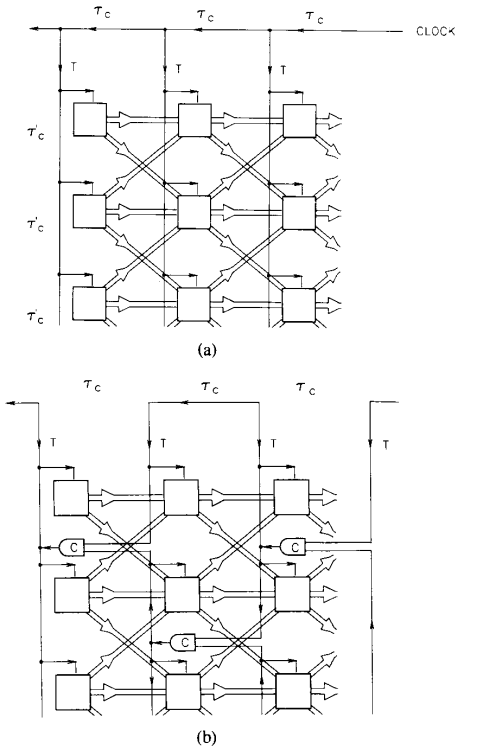

Fig. 23. Clock distribution systems for a quasi-uniform two-dimensional circuit. (a) The simplest system. (b) A possible system with the clock skew correction.

C. 2-D Waves and Clock Skew Correction

The similar timing schemes can be also used for quasi-uniform two-dimensional RSFQ structures. For example, let us come back to the parallel multiplier shown in Fig. 20(a). We have seen that its operation requires a nearly simultaneous feeding of all elementary cells of its vertical columns by clock pulses, with each column being fed somewhat later than its right neighbor.

Fig. 23(a) shows the simplest way for the appropriate timing of a general 2-D structure of this kind (with quasi-local signal connections). This counterflow scheme organizes a leftward motion of a clock wave, which induces a rightward motion of the signal waves. For operation with arbitrary elementary cells, not only (6) but also the condition

$$n\delta\tau_c' \ll \tau \tag{7}$$

(where $\delta\tau_c'$ is an average irregularity of the traversal delay τ_c') should be satisfied. For long operands, this condition can limit the clock frequency significantly.

For such structures, there are better ways to ensure the clock wave front linearity (in other words, to correct the "clock skew"). One of the ways is shown in Fig. 23(b). Here *C* denotes a *coincidence junction*. Within the RSFQ convention this is a circuit that provides its output SFQ pulse as soon as both its inputs have been fed by such pulses. (Note that by definition this circuit is *not* the elementary RSFQ cell, because it is not timed from a certain terminal. If one likes it another way, it is the DRO register cell for its input arriving earlier, which is clocked by the input arriving later.) Fig. 24(a) and (c) show a possible structure of the coincidence junction and results of its numerical simulation; for basic characteristics of this circuit, see Table II. Note that the circuit is designed in a way that insures its self-reset to the "00" state (with both interferometers reset to their "0" state) right after turning on the dc supply.

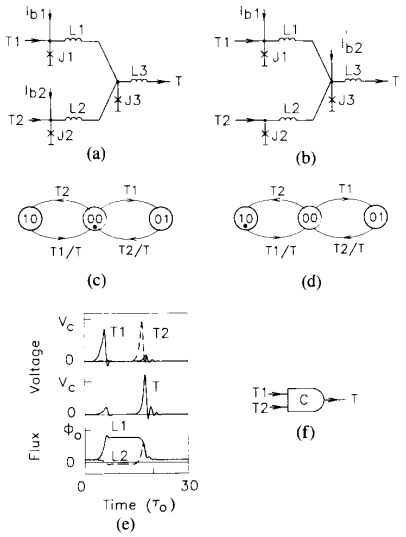

Fig. 24. Coincidence junction. (a) A possible equivalent circuit with the initial "00" state. (b) Its version with the initial "01" state. (c), (d) Corresponding Moore diagrams. (e) Dynamics of the circuit. (f) Its notation [29], [34].

Coming back to Fig. 23(b), one can see that the coincidence junctions compensate possible parasitic delays of the clock pulses in the horizontal lines (due to, say, imperfections of the layout) and thus cancel the limitation expressed by (7).

D. Hand Shaking

All previous discussion of the RSFQ circuit timing assumed that the clock pulses are generated by some circuit external to those under consideration. This way is possible for relatively small circuits where all time delays of the pulse propagation from a clock generator can be provided with an accuracy better than the clock period τ. For most circuits, however, another approach turns out to be preferable. In this approach, each fragment (cell or block) of the system is complemented by a special circuit that generates the clock pulses for its signal correspondents.

Fig. 25(a) shows such a circuit for a shift-register type structure. Let the register be filled up by a string of data and all the coincidence junctions have received their acknowledgment (ACK) pulses. In the following schemes the correspondent inputs of the coincidence junctions will be marked by 1. (If one needs to ensure the correct operation of the circuit immediately after the first turning on of the whole device, he should use the conjugate junction version which is shown in Fig. 24(b). This circuit self-resets to its "10" state with the flux quantum trapped in the L1 loop.)

The cell is waiting for the arrival of the SEND pulse signaling that the receiver cell is reset and hence ready to accept the new data. This pulse triggers the coincidence junction, which first

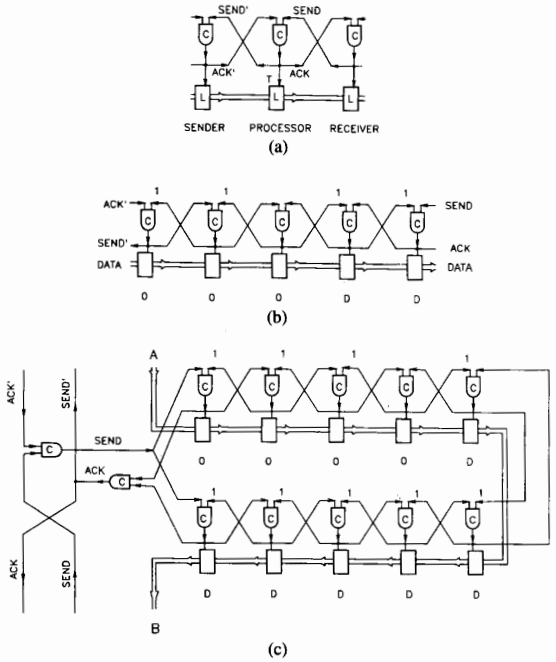

Fig. 25. Hand-shaking approach to the clock pulse distribution. (a) Timing of an elementary cell [28]. (b) The elastic pipeline mode of operation. (c) The fixed-period-delay (or Z^{-1}) register using the latter mode. D and 0 denote cells with and without data, respectively.

produces the clock pulse T for its native cell and thus forces it to send its output signal to the receiver. Simultaneously, this pulse is duplicated as the ACK signal necessary to set up the coincidence junction of the receiver and (after an appropriate delay τ_c) as the SEND′ signal for the next (sending) cell. As a consequence, the whole data string will be eventually shifted by one step to the right. This counterflow operation mode can be used, for example, for timing the shift registers formed by N and FA cells of the serial multiplier (Fig. 18(a)) and vertical columns of the parallel multiplier (Fig. 20(a)).

The same clock distribution system can operate in the "load" mode similar to that of the circuit shown in Fig. 21(b). Let the shift-register-structure be initially empty, and let all the coincidence junctions have been sent their SEND pulses. Now if a signal and the accompanying ACK′ pulse are fed into the left end of the whole structure, the arising clock wave pushes the data bit through all the structure. This mode can be employed, for example, for timing the shift register formed by cells R of the serial multiplier (Fig. 18(a)).

Even more interesting is a combination of these two operation modes when the data string is shorter than the register and thus occupies its right section of some length. (The coincidence junctions are to be set up correspondingly, with the boundary junction in its "00" state; see Fig. 25(b).) Now each SEND pulse fed into the right end of the structure induces a shift of the data string by one step to the right, decreasing the data string length. On the contrary, an ACK′ pulse fed into the left end (together with the data bit) induces a rapid loading of the bit to the rightmost empty cell of the register, joining it to the data string, which is not shifted during this operation.

It is clear that this "*elastic pipeline*" mode is very convenient for design of very natural superfast blocks. As the simplest

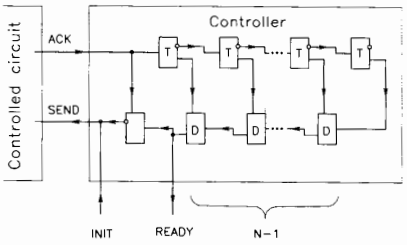

Fig. 26. A simple RSFQ clock controller providing a single train of N clock pulses.

example, if the elementary blocks in Fig. 25(b) are merely the single-bit register sells D (Fig. 7), this circuit can serve as the *first in–first out* (FIFO) shift register. Its total length (including forward and reverse branches) should be somewhat larger than the data string length. Fig. 25(c) shows a slightly more complex circuit of the similar single-bit register cells. One can be convinced that this block, the Z^{-1} *register*, provides the data delay by a fixed number of clock pulses. Despite a possibly very large length of the block, there is no chance that parasitic delays of the clock pulses can disturb its operation (of course, if (6) is fulfilled for all *local* delays).

If one closes the Z^{-1} register input and output through a simple multiplexer/demultiplexer circuit, he gets a circular register that can also serve as the serial access memory.

E. Clock Controllers

All the RSFQ structures we have discussed up to now (including the most "closed" one, shown in Fig. 25(c)) are still to be fed by ultrafast trains of the picosecond clock pulses. One could imagine that these trains should be generated by some clock generator, which in particular determines their period τ that should satisfy (6) for all the cells of the timed circuit.

This conclusion is only correct for the simplest clock distribution systems (Figs. 21 and 23), and this is one of the reasons why they are not quite convenient. The hand-shaking approach eliminates this need and allows one to use clock *controllers* rather than *generators*: the former device predetermines only the number and sequence of the pulses rather than their period.

As a simple example, Fig. 26 shows a possible controller for an RSFQ circuit that needs a single train of N clock pulses. Its operation is started by an external signal INIT, which is passed to the controlled circuit as the first SEND pulse. After the termination of the first operation period, the circuit sends the acknowledgement ACK to the controller which uses it to generate the second SEND pulse, etc., until all N necessary pulses have been produced (the last pulse triggers the READY bit signaling that the whole operation has been completed). Note that the structure of this controller enables it to provide a very fast (few-picosecond) SEND response to each ACK input, independent of N (i.e., of the length of the structure).

One can see that the period τ between the pulses is determined by time delays in both the controlled and controlling circuits, and thus is automatically adjusted to the shortest value that is acceptable for the correct operation of the whole device. Hence the hand-shaking approach allows one to omit τ from (6) and take care exclusively of the correct relation between (local) values of δ and τ_c during the RSFQ circuit design.

Concluding the discussion of the hand-shaking approach, it is necessary to note that it is in fact quite common for communications in modern asynchronous computer circuits (see, e.g.,

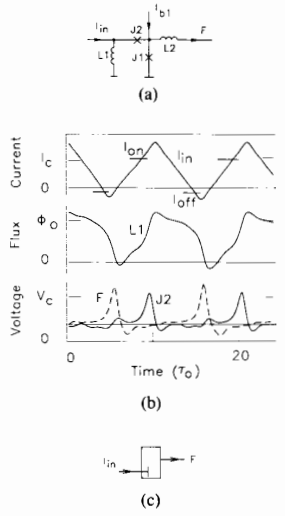

Fig. 27. Asynchronous dc/SFQ converter. (a) Equivalent circuit. (b) Dynamics. (c) Notation [26].

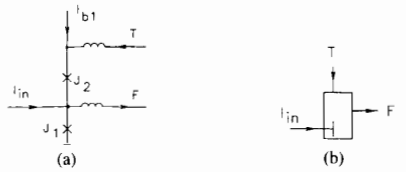

Fig. 28. Timed dc/SFQ converter. (a) Equivalent circuit. (b) Notation.

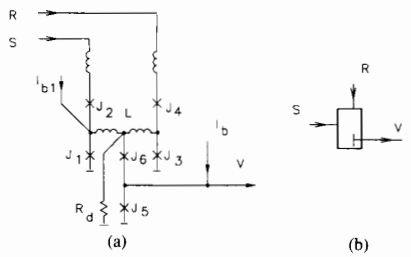

Fig. 29. SFQ/dc converter. (a) Equivalent circuit. (b) Notation.

[10]), and even the structure of our basic timing circuit (Fig. 25(a)) is formally similar to that used in the semiconductor electronics; see, e.g., fig. 2 of [35]. Thus one can borrow quite a few recipes suggested by semiconductor self-timing discipline for a design of more complex RSFQ circuits.

The really new feature that the RSFQ circuitry brings into this discipline is a common use of the hand-shaking approach on the lowest (single-bit) level because of enormous operation speed of these circuits and hence their high requirements imposed on the clock delays (note recent attempts to apply this approach at an almost similarly low-scale level in the high-speed semiconductor circuits [35]). On the other hand, the natural internal memory of the RSFQ cells (including the coincidence junctions) makes the single-bit hand-shaking not excessively hardware-consuming.

VI. Possible RSFQ Systems and Their Performance

A. dc/SFQ and SFQ/dc Conversion

Proceeding to a discussion of possible digital and analog/digital systems that could use the RSFQ technology, one should take into account the following grave fact: *the picosecond SFQ pulses can hardly be passed between the IC chips*, at least using the present-day packaging techniques (see. e.g., [36]). Hence the information should be transferred from the SFQ form into the usual dc-voltage form before being passed between the chips, and then converted back into the SFQ.

Fig. 27(a) shows a simple asynchronous dc/SFQ converter based on the two-junction interferometer. If its input current I_{in} is increased beyond a certain threshold value I_{on}, the critical state of the junction J1 is achieved, and the standard SFQ pulse is generated (Fig. 27(b)). In order to restore the initial state of the interferometer, I_{in} should be now decreased below a value I_{off}. The reset of the circuit is accompanied by generation of the SFQ pulse across another junction (J2), which does not penetrate to the circuit output.

The major disadvantage of the converter is that its output pulse is not synchronized with the clock period of the following RSFQ circuitry. Fig. 28 shows how this drawback can be avoided. In this circuit, which is similar in structure to the buffer stage (Fig. 5) but operates as a balanced Josephson-junction comparator [11], [37], the input dc current determines whether the clock pulse T triggers the 2π-leap in the junction J1 and hence whether an output pulse is developed across this junction just after arrival of T, or not.

Fig. 29(a) shows a possible structure of the SFQ/dc converter. Its heart is the RS flip-flop formed by interferometer (J1, J3, L), connected to an additional pair of the Josephson junctions (J5, J6), quite similarly to the N cell (Fig. 11(a)). There are, however, minor differences between the two circuits: in the SFQ/dc converter the junction pair is externally shunted by an additional resistor R, and the bias current I_b is considerably larger than that in the cell N. Due to these differences, switching of the basic interferometer to its "1" state leads to the resistive state of the junctions J5 and J6 (accompanied by continuous Josephson oscillations), i.e., to the appearance of a nonvanishing dc voltage V at the converter output. An important advantage of this converter is its self-resetting feature: switching the basic interferometer to its "0" state by a resetting (typically, clock) pulse R leads to a rapid decay of the output dc voltage. Internal time delay of the converter is relatively long on the τ_o scale, but considerably shorter than that of any feasible circuit accepting the developed dc signal.

The dc/SFQ and SFQ/dc converters have been tested experimentally [26] to operate at frequencies well in excess of 100 GHz, despite their implementation with a relatively primitive 5-μm technology. In these experiments, the asynchronous dc/SFQ converter was connected by the SFQ transmission line (Fig. 3) to the SFQ/dc converter combined with the T flip-flop, i.e., the single-bit section of the binary counter (Fig. 30). As a result, when the circuit was fed by a triangle waveform (top trace in Fig. 31), a square waveform was developed at its output (the middle trace in Fig. 31) although no detectable waveform appeared across the transmission line (the bottom trace), because the experimental setup could not register the picosecond SFQ pulses carrying the signals between the converters. These experiments have shown that the dc/SFQ and SFQ/dc converters can operate with more than $\pm 30\%$ parameter margins, in good agreement with the simulation results (Table II).

One might have noticed that the output voltage of the SFQ/dc converter is still low, which makes high-speed testing even more

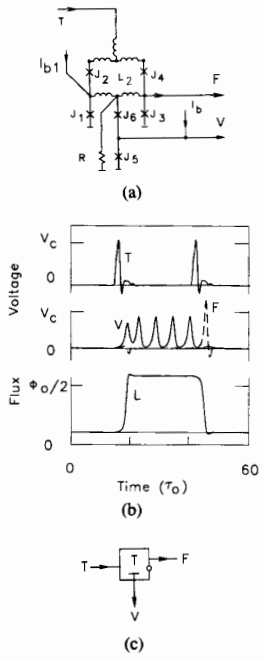

Fig. 30. SFQ/dc converter combined with the T flip-flop (c.f. Figs. 8, 29). (a) Equivalent circuit. (b) Dynamics. (c) Notation [26].

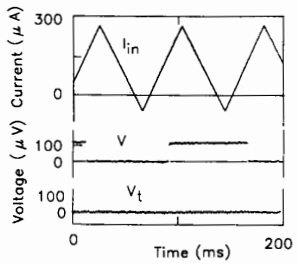

Fig. 31. Experimental oscillograms of operation of a test circuit containing the dc/SFQ and SFQ/dc converters connected by the SFQ transmission line [27].

difficult than that in latching logic. This drawback can be easily removed at the price of decreasing the upper frequency of the conversion. In this case one can use as an output stage of the converter a well-known unlatched dc biased flip-flop (or huffle) based on underdamped Josephson junctions [76]. The operation of the huffle has been demonstated with the output voltage as large as 2 mV and the upper frequency as large as 0.5 GHz by using 5-μm design rules Pb-alloy technology [77]. The design of the SFQ/dc converter based on this idea is now in progress.

B. A/D Converters

A/D converters seem to be the simplest and hence the most immediate application of the RSFQ technology. The reasons for this are similar to those listed in the Section I: the extremely high switching speed of the Josephson junctions determines a very short (picosecond-scale) aperture time τ_a of the converters using them. By a proper design of the converter, this short time can be traded for either a better accuracy ϵ or a larger signal frequency F_{max}, according to the general relation [38]

$$F_{max} = \epsilon/\pi\tau_a, \qquad \text{i.e., } \pi F_{max}\tau_a = 1/2^n \tag{9}$$

where $n = \log_2(1/\epsilon)$ is the number of correct bits. Another important advantage of the Josephson junctions, which allows hardware-saving designs of the converters, is the natural 2π-quantization of the Josephson phase ϕ (equivalent to the ϕ_0-quantization of the magnetic flux).

Two types of the Josephson-junction A/D converters have been developed during the last decade: *parallel* and *serial* (or *counter-type*) ones; for a recent review, see [38]. (Compensation-type versions of the serial A/D converters are usually referred to as the *digital SQUID's*; we will discuss them in the next section.) The former converters are usually believed to provide the highest F_{max}. However, they need a simultaneous delivery of ultrafast sampling waveforms to each of their n samplers, and an extremely high ($\sim \epsilon$) precision of their comparators and analog input signal dividers. Both factors do limit the effective aperture time, so that the experimentally demonstrated performance of the converters (say, $F_{max} \cong 100$ MHz for $n = 6$ bits) are worse than that evaluated by numeric simulation without taking into account mentioned above parasitic factors (say $F_{max} = 5$ GHz for $n = 5$ bits) or achieved at their semiconductor commercially available counterparts (say $F_{max} \cong 1$ GHz for $n = 5.2$ bits) [38]. Despite some recent reasonable suggestions [39] that can help to improve the performance, we believe that much better prospects exist for the serial or parallel-serial converters.

A possible core of the latter devices, the so-called *ripple counter* based on overdamped Josephson junctions, was proposed more than a decade ago [40] (see also [41]). Its practical application was, however, pending until a way could be found to carry out an ultrafast readout and preliminary processing of the digital output of the device. The RSFQ circuits open such a way. In order to demonstrate that, a test RSFQ circuit picking up information from a modified version of the ripple counter has been tested recently [28].

The quantizing part (comparator) of this A/D converter is the usual two-junction interferometer (J1, L, J2 in Fig. 32(a)). The input analog signal current I induces a proportional magnetic flux $\phi = MI$ applied to the interferometer. If the flux is constant, no SFQ pulses appear at the outputs. If the flux is increased in time, and crosses a level $\Phi_{on} + k\Phi_0$ (with an integer k) the junction J1 reaches its critical state and the SFQ pulse (a "ripple") is triggered in this junction. Thus the SFQ pulse rate at the direct output of the counter equals $|\dot{\Phi}|/\Phi_0$ at $\dot{\Phi} > 0$. At $\dot{\Phi} < 0$, this junction is silent, but junction J2 develops a similar amount of pulses at the reverse output of the converter. So the comparator produces 1-bit numbers (pulses), which are a differential code of the analog signal Φ. To get the usual binary form of the signal, these numbers should be counted (integrated) as positive ones for direct output and as negative for reverse output.

In order to do that, the RSFQ binary counter, consisting of a series of T flip-flops (Fig. 8), is connected to the direct output of the comparator and an RSFQ transmission line (Fig. 3) to its reverse output. The SFQ splitters (Fig. 4) and confluence buffers (Fig. 6) feed the reverse-output pulses into each T flip-flop. As a result, each direct-output count increases the counter contents by 1 ("$0\cdots01$" in binary code), while each reverse-output count, by -1 ("$11\cdots1$" in binary code). Thus the desired subtraction is achieved, so that the contents of the binary counter represent a binary code of Φ/Φ_0. The code could be read out

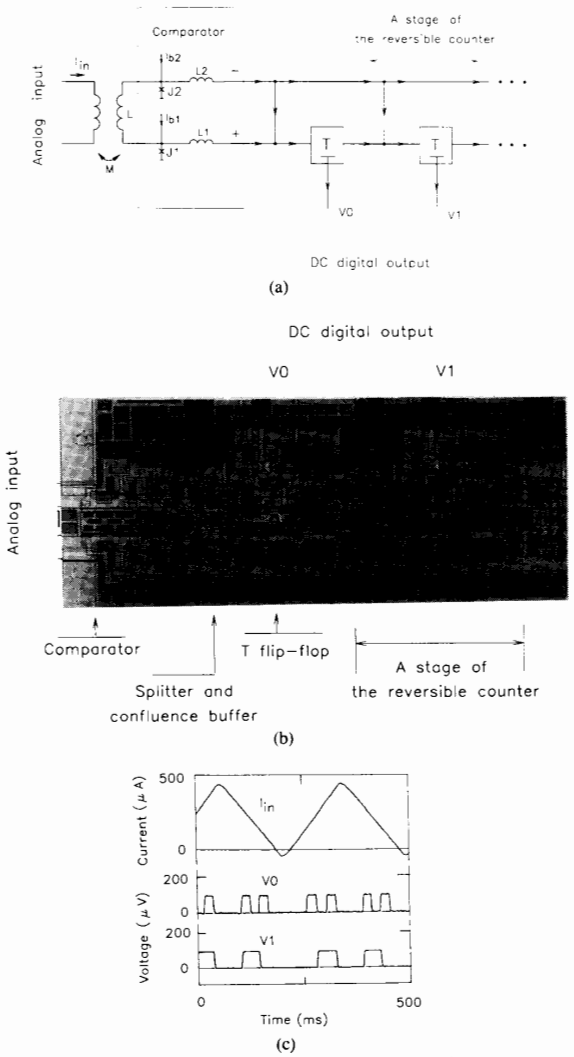

Fig. 32. Test RSFQ circuit with an asynchronous serial A/D converter and a 8-stage reversible binary counter with SFQ/dc converters for each bit. (a) General structure. (b) Microphotograph of the circuit. (c) Oscillograms of operation of the first two stages. (Photo presented by courtesy of Dr. V. Koshelets.)

continuously using the SFQ/dc converters combined with each T flip-flop (Fig. 30). Fig. 32(b) shows the whole circuit implemented using a 5-μm all-Nb technology and containing 169 Josephson junctions and 300 resistors, while Fig. 32(c) illustrates operation of its first two stages (for more details, see [28]).

A more complex processing of the output signal of this converter is, however, impeded by a major disadvantage of the ripple counter: its output pulses are not synchronized with the clock pulses of the following RSFQ logic stages. As a result, the pulse can fall into the "gray zone" between two neighboring clock periods, and thus either abandon counting or be counted twice.

This problem can be solved [33] using the timed A/D converter (Fig. 33). In its essence the comparator (Fig. 33(b)) is the

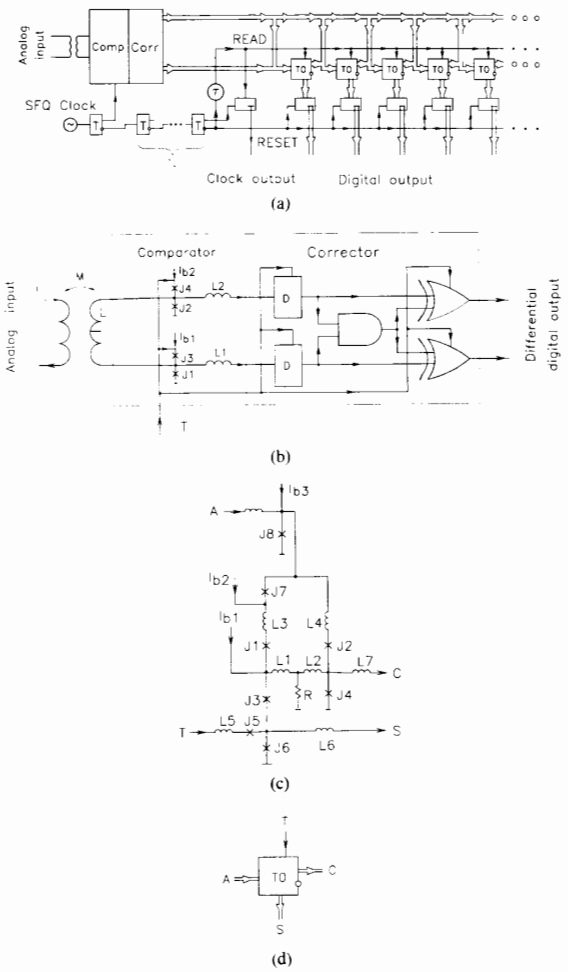

Fig. 33. Serial timed A/D converter. (a) General structure. (b) Equivalent circuits of the comparator and corrector blocks. (c) Equivalent circuit of the block *TO*. (d) Its notation [33].

two-junction interferometer (J1, J2, L), formed by lower junctions of two clocked comparators (c.f. Fig. 28). Its operation is similar to that of the ripple counter, with the exception that all the SFQ pulses are triggered by the clock pulses T and thus are tightly bound in time to the clock pulse arrival moments.

A minor remaining problem is that sometimes both direct-output and reverse-output pulses can be generated during one clock cycle. This is why the digital part of the device should start with the corrector (Fig. 33(b)) containing an AND gate combined with two DRO register cells D, and two XOR cells. It is straightforward to check that if the SFQ pulse arrives from one channel alone, it is passed by the corrector to the corresponding output, but arrival of the counts from both channels result in no output at all. The latter outcome also leads to the correct result eventually, because the number of pulses coming from the direct and reverse channels should be later subtracted anyway.

Fig. 33(a) shows the digital part of the simplest version of the converter. The circuit is timed by a continuous train of the SFQ pulses (it can be generated by just a single overdamped Josephson junction, dc biased slightly above its critical current). The

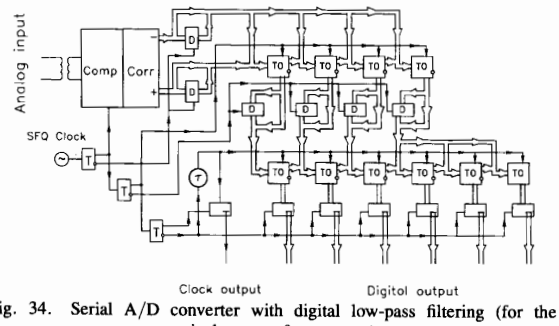

Fig. 34. Serial A/D converter with digital low-pass filtering (for the particular case of two stages).

output pulses from the direct and reverse channels of the comparator-corrector unit arrive at the corresponding inputs of an n-bit reversible counter generally similar to that discussed earlier (Fig. 32). Its contents could be read out continuously (as Fig. 32(a) shows), but if this operation is slow (i.e., limited by a relatively large time of the dc signal transfer from the converter chip), then several least significant bits could be already wrong because of simultaneous change of the signal. Fig. 33(a) shows how this drawback can be avoided. The asynchronous T cells are replaced here by clocked *TO* cells (Fig. 33(c)). This cell is a T flip-flop with an additional DRO circuit for the complementary-code readout S (Fig. 34(b)), so that the register as a whole is just a binary counter with the parallel destructive readout in the complementary code. The readout clock pulse train is running along the counter with the same speed as the data, and destructively reads out the counter contents, corresponding to the input signal value at a certain instant, to the output register of the SFQ/dc converters. So the counter stores the variation of its inputs during the readout period $\tau' = 2^N\tau$. Its output dc signals can be read out relatively slowly (with a frequency of the order of F_{max}). The clock pulse arriving along the RESET line clears the output register just before reading in the next data from the counter.

To get an idea of a possible accuracy of such a converter, let us note that its output bit number can be restricted to $N = \log_2(F_{max}\tau)$, and that the clock period τ is limited from below by the operating speed of the slowest RSFQ stage. For example, for a feasible value $\tau = 10$ ps (c.f., Tables I and II) one can get $N \cong 10$ correct bits of a signal with the upper frequency $F_{max} = 100$ MHz (or $N = 6.5$ bits with $F_{max} = 1$ GHz). These figures (reasonably good) do *not*, however, approach the ultimate performance limits of the RSFQ circuitry. There are two ways to improve the accuracy of conversion.

The first one is using a well-known oversampling technique based on sampling of a signal at a rate well above the Nyquist frequency (see, for example, [75]). The error introduced by the quantizer is spread out the entire frequency band from zero to the sampling frequency $1/\tau$. Quantization noise above the signal band is then removed with a digital decimation filter wherein the signal is resampled at the rate $2F_{max}$. A possible algorithm of this filtering is just a successive replacement of even counts by mean values of the even and the neighboring odd counts. Then odd counts are dropped (decimated) from further processing.

Fig. 34(a) shows a possible RSFQ circuit performing such a filtering. Here the output signals of the comparator-corrector unit feed the register of four *TO* cells (Fig. 33(c)). The subtraction of the direct and reverse counts is achieved again by feeding all stages of the counter in parallel by the reverse-output pulses (c.f., Figs. 32(a) and 33(a)). Averaging of two consequent counts is achieved by a delay of each count for one clock period in a simple register cell D (Fig. 7), and by addition of its contents to the next count. Decimation of the redundant counts is achieved simply by the (destructive) reading out of the contents of the counter only once for two clock periods.

These contents are sent into the similar but 6-bit binary counter, again with signal averaging by additional D cells. After every four clock periods, similar operation is fulfilled with the contents of these latter counters, etc. (Note T flip-flops in the clock distribution line, providing division of the clock pulse frequency by two on each stage.)

One can be readily convinced that each binary counter provides the correct differential digital code of the input signal (except all odd stages yield this information in the complementary code). The further right is the counter, the larger is the number of output bits (by two bits per stage) and the lower is the output frequency (by a factor of two per stage). An analysis of the device operation shows [33] that $N/2$ least significant bits of its output (where N is the number of stages) present the quantization noise and should be neglected, while the remaining half of the additional N bits are correct and present the accuracy gained due to the signal averaging at the same output code frequency F_{max}. This means that $\cong 15$ bits rather than $\cong 10$ bits would be correct in the example discussed above ($F_{max} = 100$ MHz).

Note that the parallel implementation of the decimation filter discussed above works well for several first stages where clock frequency is high enough. For the next stages the serial way of digital processing is less hardware consuming [33].

The second way to improve the accuracy is as follows. Recall that both the comparators (Fig. 33(b)) that feed the decimation filter can be considered as 1-bit A/D converters with differential coding. Each of these comparators could be replaced with a parallel A/D converter (comprising 2^p comparators), which produces p-bit differential code of the analog signal [33]. It is evident that this way increases the total conversion accuracy by p bits. Computer simulation of the device employing such a technique proved its steady operation at least for $p = 2$ with the clock frequency *no less* than that of the clocked comparators shown on Fig. 33(b) [33]. The two additional bits lead to the total accuracy of $\cong 17$ bit for $F_{max} = 100$ MHz (or $\cong 12$ bit for $F_{max} = 1$ GHz).

Formal substitution of the resulting accuracy and frequency to (9) (which does *not* take the averaging feature into account) yields the effective aperture time τ_a in a 0.1-ps range. To the best of our knowledge, this unique performance cannot be challenged by any other physical device, either tested or projected. Its origin is the ultrahigh sampling/processing frequency available in the RSFQ circuits.

C. Digital SQUID's

The effective digital filtering described above can also be used for development of digital SQUID's that would combine high sensitivity of their analog version [8] with a much higher slew rate and a virtually unlimited dynamic range [33].

Consider an example shown in Fig. 35. The usual analog dc SQUID (J1, J2, L1) senses the current flowing in the input coil L2 of its dc transformer, and produces proportional changes of the its output dc voltage V. After a moderate low-pass filtering, this signal controls the SFQ-clock driven comparator formed by junctions J3–J5 (c.f., Fig. 28). If the dc signal I is above a

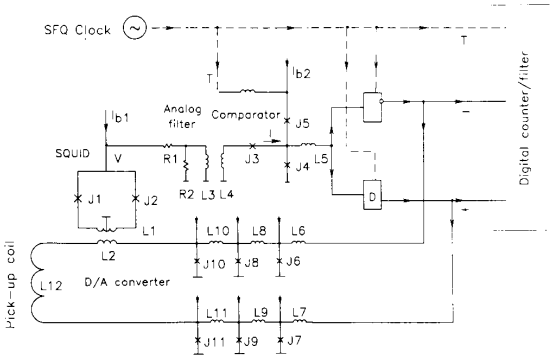

Fig. 35. A possible structure of the compensation-type low-frequency A/D converter (the "digital SQUID") [33].

certain threshold, the clock pulse T induces the 2π-leap in junction J4, which is then applied to the clocked inverter and the register cell D. As a result, an SFQ pulse appears at the direct digital output, and it is also injected to the positive (bottom) arm of the feedback loop. After passing the Josephson transmission line (J7, J9, J11; c.f. Fig. 3), the single flux quantum is injected to the pick-up coil of the SQUID. The polarity of the injection ensures *reduction* of the input flux applied to the dc SQUID by $\beta\Phi_o$, where $\beta \ll 1$ is the transfer factor. This injection of a single flux quanta would continue each clock period until the analog output V of the dc SQUID reduces the input current I of the comparator below its threshold. As a result, the junction J5 rather than J4 would be switched each clock period, leading to supply of the SFQ pulse to the reverse digital output and insertion of the single flux quantum to the negative (top) arm of the feedback loop. Hence the threshold will be approached from the either side.

This on-chip negative feedback is generally similar to that described by the Fujitsu group [73] with an important exception that in the RSFQ version the clock frequency f can be extremely fast (well beyond 100 GHz, the figure to be compared with 0.5 MHz) in [73]. As a result, the slew rate $s = \beta\Phi_o f$ can be as large as $\sim 10^9\ \Phi_o/s$ (we have used a realistic value $\beta \cong 10^{-2}$ which would make the additional quantization flux noise $\delta\Phi = \beta\Phi_o/f^{1/2} \cong 3 \times 10^{-8}\phi_O/\mathrm{Hz}^{1/2}$ of the device less than the intrinsic noise of the best practical dc SQUID's).

Note that the device shown in Fig. 35 has a virtually unlimited dynamic range, and that the static input inductance of the device is infinite, thus allowing large and/or remote pickup coils. The SFQ digital output of the device presents the time derivative of the signal, just as in the A/D converters considered above, so that its counting/filtering can be fulfilled just as Fig. 34 shows. The number M of the consequent sections of the filter should be sufficient to reduce the output signal frequency $f_{\mathrm{out}} = f/2^M$ to a value permitting its pickup by the semiconductor electronics for a further processing. For a quite feasible value $f_{\mathrm{out}} \sim 10$ MHz we would need M $\cong$ 14 stages and hence some $\sim$ 4000 Josephson junctions on the chip. This number may be reduced by a factor of two or tree with the help of serial rather than parallel processing at the last (longest and slowest) stages. The remaining complexity can be readily traded off for performance by reduction of f and s; ultimately, one can use external clock and no SFQ counting/filtering at all, thus reducing the number of junction to 15 or so. We believe, however, that there are good prospects for the full-scale full-performance device as well.

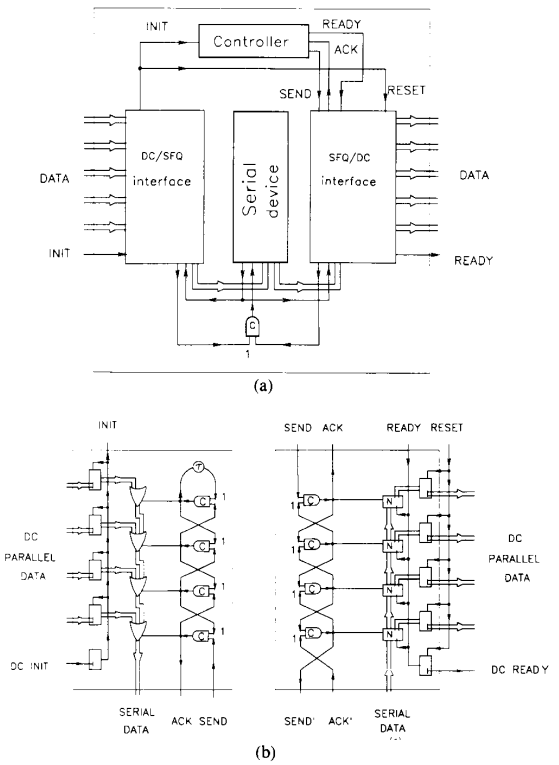

Fig. 36. Serial RSFQ chip with the serial data bus. (a) General structure. (b) Its dc/SFQ interface. (c) Its SFQ/dc interface.

D. Digital Signal Processing

Fig. 36 shows a possible general structure of an RSFQ digital chip. Because of the interchip communication problem discussed in the beginning of this section, the chip should be equipped by the dc/SFQ and SFQ/dc converter interfaces. Due to a relatively slow dc exchange rate ($\lesssim$ 1 GHz), the interface should be parallel from outside, but can be serial inside where the RSFQ circuitry enables one to achieve exchange rates well in excess of 100 GHz. Such an input parallel/serial interface (Fig. 36(b)) can be organized as a shift register consisting of the OR cells (Fig. 10) fed by the timed single-bit dc/SFQ converters (Fig. 28). The output serial/parallel interface (Fig. 36(c)) can be organized as the register of the N cells (Fig. 10) with their NDRO outputs feeding the single-bit SFQ/dc converters (Fig. 29).

The other key components of the chip are the digital device itself and a clock controller. Let us consider the operation cycle of the device as a whole, supposing that the hand-shaking approach (Fig. 25(a)) is applied for the clock distribution to all the cells, and that all the coincidence junctions are initially set for the counterflow (shift) mode. At first, the dc inputs should be supplied with the data to be processed. Then the clock signal INIT, which confirms relevance of the data, arrives. It is converted to the INIT SFQ pulse, which triggers the clock controller. The first clock pulse generated by the controller (see Fig. 26 for the simplest example of this block) arrives at the first stage of the SFQ/dc interface as a SEND signal. Passing the coincidence junction of the stage, this signal is duplicated as the SEND' signal for the next cell and the ACK signal coming back to the controller. The latter pulse starts a new similar clock

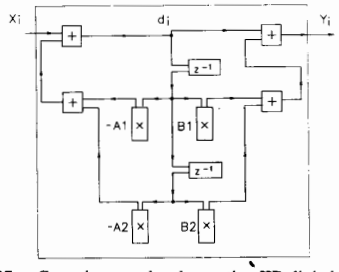

Fig. 37. Canonic second-order section IIR digital filter.

pulse, etc., so that a clock wave starts to propagate towards the signal wave. It is evident that the clock period is established at a value τ_c which is slightly in excess of the time delay δ of a *single* stage of the register (typically, a few picoseconds, see Tables I and II). Note that when/if the clock wave meets slower cell(s), this local timing scheme automatically slows its pace accordingly.

When the clock wave reaches the far end of the circuitry (the upper edge of the dc/SFQ interface in Fig. 36(a)) it is closed by a simple loop; the SEND pulse developed by the last register cell is used just as the ACK pulse fed back to the same cell after a certain (small) time delay $\Delta t \sim \tau_o$. This "boundary condition" provides the continuous clock wave flow regardless of the total length of the clock path. The operation of the device is terminated by the clock controller after it counts the proper number of clock periods. As a result, the controller stops pushing the clock wave (and hence pulling the signal wave) and sends the READY signal outside (through a single-bit SFQ/dc converter).

Note that Fig. 35(a) shows just the simplest pipeline structure (such devices are most promising for utilization of the enormous speed of the RSFQ circuitry). More complex circuits may require multiple joints of the signal and accompanying clock lines with a more complex hand-shaking protocol in the joints in order to ensure the correct signal exchange.

Now let us consider several concrete RSFQ digital chips of this type and their discuss possible performance. The simplest example is the serial multiplier (Fig. 18). Table III shows estimated performance of such a device in comparison with those for other digital technologies. One can see that the serial RSFQ device can combine a record speed with an exceptional simplicity. Even implemented with a present-day (few-μm-design-rule) technology, it will occupy only a small fraction of a standard chip area. This is why more complex devices can be even more attractive for implementation.

Fig. 37 shows a core component of another very useful device, the digital filter with a virtually arbitrary transfer function, processing a regular inflow of n-bit numbers X_i. Such a filter can be composed [42] of the second-order sections (Fig. 36). The section calculates first the linear combination

$$d_i = X_i - A_1 d_{i-1} - A_2 d_{i-2} \tag{10}$$

of the current number with two preceding numbers (so that d_i is dependent implicitly on all the former data), and then the output numbers

$$Y_i = d_i + B_1 d_{i-1} + B_2 d_{i-2}. \tag{11}$$

In the frequency domain, (10) and (11) correspond to the function

$$Y(z) = \frac{B_2 z^{-2} + B_1^{-1} z + 1}{A_2 z^{-2} + A_1 z^{-1} + 1} X(z). \tag{12}$$

Such sections can be combined to perform arbitrary linear transforms of the input data, including time-dependent transforms (provided that the numbers A_i and B_i are changed from one cycle to another).

In the RSFQ technology, the second-order section can be composed of our familiar blocks: two digital delays (Z^{-1} registers), four single-bit full adders, and four serial multipliers (Fig. 37). The last components are most complex and slow, and thus determine both the operation speed and integration scale of the section. According to Tables I and II, the section handling 32-bit numbers (and requiring only as few as some 12 000 Josephson junctions), being implemented with 2.5-μm technology, could process up to 5×10^8 numbers/s. This is why it would enable one to extend elaborate methods of the digital signal processing, developed for "acoustic"-frequencies (several–ten-kHz) [43], to "radar"-frequency signals (tens and even hundreds MHz).

Of course, this is just one example, because similarly fast RSFQ circuits can be designed for other types of digital signal processing. Nevertheless, we believe that the example shows clearly that this new technology opens unique opportunities for several areas of the applied electronics, particularly for radars and communications.

E. Computing

In contrast to digital signal processing, a universal von-Neumann-type computer is probably the worst device for implementation using the RSFQ (or any other superfast) technology. The reason is that such a device relies on frequent data exchange between the processor and memory, with the exchange rate being limited by at least the light speed (~ 100 ps per 1-cm distance). One can see that if the processor and the bulk of the memory are located on different chips (as they typically are), it leaves no hope for an over-10-GOPS productivity (per one processor).

Let us, nevertheless, estimate a possible performance of the RSFQ-based circuits of this type. A simple RSFQ microprocessor can be designed in the serial fashion (Fig. 36); it would require a serial ALU with only ~ 100 elementary cells with 4 to 15 Josephson junctions each, one serial multiplier, some 64 memory registers with 3 to 4 Josephson junctions per bit, and several tree commutators containing ~ 100 single-bit multiplexers and demultiplexers (with 7 to 8 Josephson junctions each). It leaves us with less than 5000 junctions altogether. On the other hand, an elementary analysis (using Tables I and II) shows that even with an existing fabrication technology (say, $a = 2.5$ μm) the net logic delay of the device can be as small as ~ 20 ps/bit.

True, such a formal analysis neglects the interblock propagation delays. Nevertheless, thanks to unique properties of superconducting microstrip lines (see Introduction) and the serial mode of operation of the devices under consideration, the delays can be minimized.

In fact, if the distance $\mathscr{L}$ between the communicating blocks is not very large, one can connect them by a uniformly distributed shift register with single-bit hand-shaking, operating in the elastic pipeline mode (see Fig. 25(b) and its discussion). This approach allows the receiving block to use first bits of the data before the last ones are sent. Its disadvantage is a relatively complex structure, and hence a considerable physical width, of the communication channel. As a reward, the signal propagation here produces *no additional logic delay at all*, provided $\mathscr{L}$ is not very large: $\mathscr{L} \leq n\bar{c}\delta \sim 1$ cm.

In the case of short numbers or instructions (or very far blocks) the communication channel can be simplified to consist

of just two bare microstrip lines for the data and the clock. If one provides the data line with fast (and simple) buffer registers on both its ends, one can use the hand-shaking approach on the single-word (rather than single-bit) level. It would reduce the propagation delays to just $\sim \mathscr{L}/\bar{c}$ (~ 100 ps/cm) per each n-bit operation. Comparison with the figures in Tables I and II shows that this delay is almost negligible even for distances as long as 1 cm.

These estimates show that the RSFQ technology allows one to implement, for example, an 8-bit microprocessor performing 5–10 billion register/register operations/s (including cash memory operations), or alternatively a 32-bit microprocessor performing 1–2 billion operations/s. These figures are considerably better than those achievable with other existing technologies using either semiconductors or superconductors (see, e.g., [22]). Note that a similar speed is attainable in more complex RSFQ processors as well, via usage of parallel blocks (e.g., multipliers; see Table III) for broadening the critical path bottlenecks; of course, this measure can cost a considerable increase of the integration scale.

One can justly argue that this increase of speed is virtually useless due to the much smaller speed of the intrachip communications between the microprocessor and the main memory in a standard general-purpose computer. Nevertheless, two comments can be made on this point:

i) The superfast microprocessors with an on-chip cash memory using, e.g., very compact registers shown in Fig. 22, can be extremely useful for controlling the real-time signal processors (see the previous section).

ii) The problem of the standard von-Neumann-type computer being too slow is not specific for the RSFQ digital technology, but will be met by any technology approaching the 100-GHz-clock-frequency frontier; the RSFQ circuits have just come there first. Solutions of this problem should be apparently looked for in development of new computer architectures that would make full use of the unique operation speed of the novel logic/memory circuits, and also take into account the final speed of the signal propagation on both the intrachip and interchip levels.

Special attention should be attracted to cellular automata structures with local interconnections of the cells (see, e.g., [44]). Note that most of the RSFQ blocks are just the cellular automata, either one-dimensional (see, e.g., Fig. 18) or two-dimensional (Fig. 20). Presently, most attention in this field is attracted to transputer-type systems where each cell is a complete microcomputer. Possibly, more elementary units like the RSFQ blocks could be more practical cells for operating with ultrafast hardware.

Another prospective direction of research and development is packaging. If a way could be found to allow the SFQ-pulse communication between chips, one could place a computer as a whole on the resulting "superchip." Here one could make full use of the fabulous speed of the parallel RSFQ circuitry (please have one more look on the estimated performance of the parallel-type RSFQ multiplier in Table III), and ten-GOPS computing speeds of single processor units would become a reality.

VII. Conclusion
RSFQ: Advantages and Problems

The Josephson-junction RSFQ circuits can perform the logic and arithmetic functions at extremely high (sub-terahertz) clock frequencies, just a few times lower than the intrinsic reciprocal time of the junctions employed. These circuits seem to represent the most fast digital technology available nowadays.

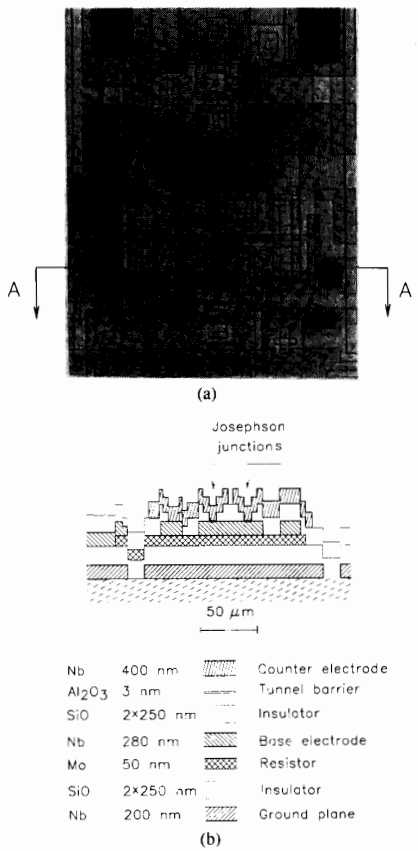

Fig. 38. Layout of a typical RSFQ elementary cell (the T flip-flop with dc converter). (a) Top view and (b) cross section of its part.

A list of other advantages of this technology includes:

i) need of only the dc power supply and only three superconducting layers (including the ground plane; see Fig. 38);

ii) large (typically more than $\pm 30\%$) parameter margins;

iii) small power consumption virtually eliminating the self-heating problems up to the VLSI level, at least for the low-T_c materials;

iv) natural self-timing, which enables one to save the ultra-high operation speed in important LSI circuits, notably the digital signal processors.

This impressive list does not mean that the RSFQ circuits are free of problems. For one, all Josephson junction technologies (RSFQ including) suffer from the parasitic trapping the magnetic flux quanta (in the form of the Abrikosov vortices) in superconducting thin films, especially that of the ground plane. Despite some recipes developed, including circuit cooling in a low-field environment, and a special ground plane patterning, the struggle against trapped flux is still more an art than the science. Our feeling is that some important reserves remain unused in this struggle, and that the problem can be solved in a radical way.

Another problem is low output voltage of the SFQ/dc converters, which urges one to develop special superconductor and/or semiconductor amplifiers of the voltage and the helium/room temperature interfaces.

There is also an important difficulty which has little to do with either physics or technology: the RSFQ idea has not yet married

an advanced Josephson junction fabrication technology, due to financial, political, bureaucratic, and apparently psychological obstacles.

The authors would be happy if this paper could help to overcome these problems.

Appendix I
RSFQ Circuit Layout Peculiarities

Layout of the RSFQ circuits is generally similar to that of the latching circuits (see, e.g., [4]–[7], [15]–[22]). Few substantial peculiarities can be traced in Fig. 38, which shows a typical RSFQ elementary cell, the T flip-flop (c.f., Fig. 8(a)). The main new feature is the external shunting of all Josephson junctions by metallic resistors R_s, necessary in order to make them overdamped, i.e., to make their McCumber–Stewart parameter [1], [11]

$$\beta_c = (\hbar/2e) I_c R_{ef}^2 C \tag{13}$$

close to 1 (a further decrease of R_s would cause an undesirable increase of the time constant τ_o; note that values of τ_o listed in Table I were calculated for $\beta_c = 1$). In any case, typical values of R_{ef} are in the few-ohm range.

Another important requirement to the shunt is its low inductance L. Calculations show that the corresponding parameter β_l, defined by (4), should be preferably less than 0.3 and by no means exceed 0.8, in order to avoid undesirable dynamic effects. In the layout, the shunt is a normal-metal thin-film strip with the length/width ratio typically close to 1. In order to reduce its inductance, the strip should pass under a part of the superconducting counter-electrode.

The second important feature of the RSFQ circuits is that they can operate without superconducting transformers (typical for the latching circuits), so that the layout is restricted to only three superconducting layers including the ground plane. As a result, the chip area A occupied by a typical RSFQ cell (expressed in the minimum feature squares a^2) is either close to, or even less than that of the corresponding gate of a latching logic; see Table II. (The experimental circuits designed and fabricated by the MSU/IRE collaboration were somewhat larger than these estimates show, because two insulating layers had to be used because of a poor quality of the insulation.)

Other factors which increase the potential integration scale of the RSFQ circuits include absence of the RF power supply transformers and most latches, required by latching logics. The present-day RSFQ circuit layout is quite convenient for implementation using one of the "all-niobium" fabrication technologies ($Nb/Al_2O_3/Nb$), first introduced by Gurvitch *et al.* [45] and then perfected considerably, mostly by Japanese laboratories (see, e.g., [15]). The MSU/IRE collaboration used several simplified versions of this technology [24], [26]–[28], [46] (with molybdenum resistors) for its relatively simple RSFQ test circuits, but for forthcoming implementation of the VLSI circuits a use of recent improvements, including planarization (see, e.g., [47]), can become a necessity.

When further progress of fabrication technology allows one to fabricate very small Josephson junctions ($S \approx 0.1\ \mu m^2$) reproducibly, a further substantial increase of the relative density (i.e., the a^2/A ratio) of the RSFQ circuits can be achieved, because a junctions of such area (with the fixed R_n of few ohms) become overdamped [48] without external shunting.

One more potential reserve is the vertical integration of the junctions [49], which is quite acceptable for the RSFQ circuits with their very small power dissipation (typically, less than 10^{-7} W/junction for 300-GHz clock frequency at helium temperatures). For example, vertical stacking of just two Josephson junctions would allow one to reduce area of the single-bit cell of the register memory (Fig. 22) to some 10 junction areas.

Appendix II
Brief Prehistory of the SFQ Digital Devices

The idea to use single flux quanta for coding the digital bits has emerged at the very early stages of studies of the Josephson effect. Probably the most influential of these early works was that by Anderson, Dynes, and Fulton [50] where the "Flux Shuttle" was proposed. This device (later implemented experimentally; see e.g., [51]) was essentially an SFQ shift register, similar in structure to the lower row of that shown in Fig. 22(a). In contrast to the RSFQ circuits, however, the shift was induced by an external *rf* drive (one position per one period).

Almost simultaneously, several other SFQ devices were proposed. In particular, the simplest single-junction interferometers ("*rf* SQUID's") have been suggested as the SFQ memory cells with destructive readout [52]–[56]. The major problem here was that of readout of the cell contents. Now we know that one can readily perform the destructive readout by picking up and processing the SFQ pulse arising across the junction during the switching, but some 15 years ago this fact was not so evident. This is why more complex cells (with typically multiquantum trapped flux) and additional NDRO circuits (converting the SFQ information to the dc form) [57] were preferred for cash memories of the latching logics [4], [22]. Similar SFQ memory cells using two-junction interferometers allow the destructive dc readout [58] and are used in the main memories in the latching-logic projects [4], [21].

In order to avoid the transfer of information from the SFQ to the dc form, several circuits capable of performing logic functions with the SFQ bits have been suggested [59]-[66]. Of those, notable is the parametric quantron (reinvented several times [59], [62], [64]), which can perform *reversible* processing of digital information and as a consequence approach the ultimate minimum of energy consumption [60], [65].

Common drawbacks of all these devices include a need in an external (typically multiphase) *rf* drive and a limited distance range of the data transfer during one clock period. (This range is determined by a specific inductance of the transmission lines and is typically of the order of the single cell size.) The reader has already seen that the latter drawback can be avoided by the ballistic transfer along superconducting microstrip lines. Historically, the first suggestion [66] was to use long Josephson junctions capable of combining ballistic transfer of the SFQ pulses with their processing, but the logic cells proposed in these works were very complex, large, and slow.

The RSFQ idea was approached closely by Arnold Silver and his collaborators who suggested [40], [41] the SFQ binary counter that was successfully tested later to operate at frequencies in excess of 100 GHz [67]. An elementary cell of this counter was identical in function to our T flip-flop shown in Fig. 8(a) (although the original design yielded rather narrow parameter margins). A perhaps even closer approach was developed by Nakajima and coauthors [68], [69] who gave examples of how ballistically moving Josephson vortices (i.e., single flux quanta) can be trapped by interferometer loops.

Nevertheless, to our knowledge the key idea of special clock pulses that would enable one to make a strict definition of the SFQ information (c.f., the RSFQ Basic Convention) and hence

to design a complete set of the SFQ logic functions had not been suggested until our first work [23].

Appendix III
Prospects for the High-T_c Superconductivity

The recent advent of the high-T_c oxide superconductors is doubtless a great scientific event that should have a significant impact on several areas of science and technology, including superconductor electronics [70], [71]. In order to use these new materials in Josephson-junction devices, however, one should solve several problems [71].

The first problem is that of reproducible Josephson junctions with suitable parameters including the I_cR_n product, normal resistance R_n, and McCumber–Stewart parameter β_c. The junctions available presently (for a recent review see [72]) are mostly overdamped ($\beta_c < 1$), and have a rather moderate value of I_cR_n (typically, several hundred microvolts at 77 K) and low R_n (typically, below 1 Ω). Their major drawback, however, is their irreproducibility, presently excluding any chance for their use in LSI circuits.

Nevertheless, due to the amount of attention attracted by this problem, progress has been quite fast, and some way(s) to fabricate decent junctions reproducibly can be found (possibly even before this paper is published). At this stage, several fundamental problems will arise, notably that of the thermal noise stability [71]. In order to keep the probability of thermal-noise-induced errors low enough, the ratio of the Josephson coupling energy $E_J = \hbar I_c/2e$ to the fluctuation energy scale k_BT should be large enough (typically, of the order of 500). For helium temperatures the resulting condition ($I_c \gtrsim 100$ μA) can be readily fulfilled. For a stable nitrogen-temperature operation, however, the critical current should be rather high ($I_c \gtrsim 2$ mA).

Currents so large cause two undesirable effects: junction self-heating and a need for very low inductances. It is easy to be convinced (see, e.g., Likharev *et al.* in [70]) that the former effect makes the latching logic circuits impractical at nitrogen temperatures. For the RSFQ circuits the energy dissipation also grows, but to a lesser extent, leading to figures close to 3×10^{-18} J/bit. For a VLSI circuit with, say, 3×10^5 Josephson junctions operating with a clock frequency of 300 GHz, one estimates a power dissipation of ~ 0.1 W. Dissipation in the bias resistors increases this figure to ~ 3 W. Such a power still can be removed from a 1-cm^2 chip by liquid nitrogen without forbidding overheating [70].

The latter problem of low inductances is more severe. We have already mentioned that loops in the RSFQ circuits typically should have inductances β_l from 3 to 10. For the above value of I_c one gets the L from 0.5 to 1.5 pH. For the smallest penetration depth $\lambda \simeq 0.2$ μm available for the high-T_c superconductors at 77 K, this fact means that the smallest loop should have not more than ~ 3 lithographic squares connected in series (an insulation thicker than $\sim \lambda$ would further reduce this figure). As one can see in Fig. 38, this limitation makes the layout design very hard. Cooling to intermediate temperatures (say, ~ 30 K) would relax this limitation significantly. Note that this evaluation is correct only for the unshunted nonhysteresis Josephson junction. Alternative situations of using shunted hysteresis junctions is less realistic because of similar problem with shunt inductances (see Appendix I).

Thus one comes to the preliminary conclusion that an acceptable solution of the Josephson junction fabrication problem could make the nitrogen-temperature-operated RSFQ circuits feasible. One can argue [71], however, that in devices so complex and so unique in their performance as the VLSI RSFQ circuits, the cooling is far from being the main concern. The authors believe that when such digital devices are implemented, they would readily find several application niches even if they required the helium cooling. Transfer to the the high-T_c materials would apparently require a much longer period.

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