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RESISTIVE SINGLE FLUX QUANTUM LOGIC FOR THE JOSEPHSON-JUNCTION DIGITAL TECHNOLOGY

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Introduction

The Josephson logic systems reported earlier were based on one of the two following physical principles. The first possibility is to code information by the magnetic flux trapped in superconducting loops; presently the single flux quanta (SFQ) $\Phi_0 = h/2e \approx 2.07 \cdot 10^{-15}$ Wb are used in most devices[1-8]. The basic drawback of these SFQ devices is that the magnetic flux suffers a nonvanishing drop along even a superconducting transmission line. As a result, the information coded in this way can be transferred to few neighboring logic cells during a single clock period. This property is hardly compatible with the traditional computer architectures.
The second way is to present information by the voltage across the Josephson junction. Such "resistive" devices are used in most resent developments of the superconducting logics[9-12] and are compatible with the traditional architectures. Its major disadvantage is that the time $\tau_{R \to S}$ necessary for the junction reset from its resistive (R) to superconducting (S) state is rather large (up to 1 ns)[13] so that the minimum clock period ($\tau_c = \tau_{S \to R} + \tau_{R \to S}$) turns out to be larger than that of the modern semiconductor gates.
The purpose of this work is to demonstrate another way to represent and process digital information in the superconducting electronics, which excludes disadvantages of the above principles.

Basic Principle

In our "Resistive Single Flux Quantum" (RSFQ) logic system the information is stored in the form of single flux quanta but is transferred in the form of single voltage pulses of the area

$$\int V(t)\,dt = \Phi_0 \,. \qquad (1)$$

In contrast with the earlier proposals[4-7] to use such pulses in logic circuitry, we present the logic unity (zero) by presence (absence) of the pulse during a period between two consequent timing (T) pulses. The latter pulses are similar in area (1) and shape to the signal ones, but are transmitted along separate lines.[17]
As a simple illustration of our principle consider a circuit (Fig.1) perfoming the Boolean function $F = ((\overline{A + B}) + C)D$. The circuit consists of NOT, OR and AND gates interconnected by buffer stages. Each gate has signal inputs S_i and a timing input T. All these inputs are supplied by the single voltage pulses (1). Signal pulses can change the internal state of the gate independently of the exact time of their arrival (within the given period between the timing pulses). The timing pulse reads out the resulting internal state of the gate, i.e., induces a single pulse of the same area (1) at the gate output in the case when the performed logic function is equal to unity.

System of Logic Gates

Figures 2 and 3 show possible realization of components of the above circuit (Fig. 1). The buffer stage (Fig. 2a) is close in structure to that discussed earlier ; it provides unilateral transfer of the pulses (1) between the logic gates with the simultaneous regeneration of these pulses. The regeneration is provided by dc-biased non-hysteretic (low-β_c) Josephson junction J_1 which performes a 2π-leap of its phase ϕ triggered by the input pulse. Series connection of the buffer stages forms a neuristor-type transmission line capable to transfer information to unlimited distance along an integrated circuit with the velocity approaching that of light. Information multiplication can be readily arranged (Fig. 2a) and channeling of pulses from two lines to one can be provided by simple connection of the outputs of the similar buffer stages.
Figure 2b shows that the logic gate OR can be designed on the basis of a symmetrical two-junction superconducting quantum interferometer flux-biased by $\Phi_0/2$ and hence possesing two similar stable states. An input pulse S_i arriving first in time changes the initial state of the interferometer while the following signal pul-

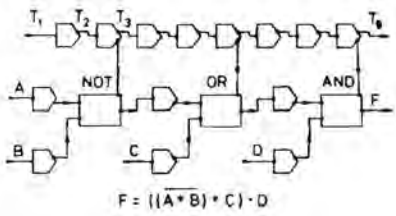

Figure 1

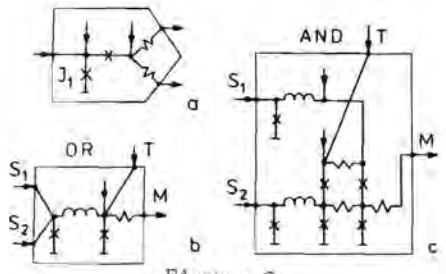

Figure 2

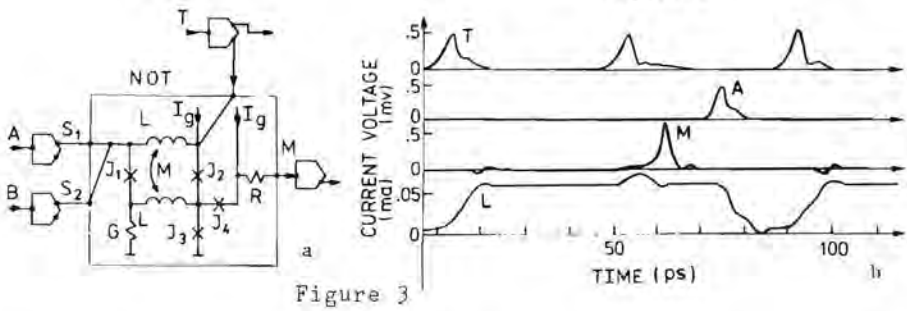

Figure 3

se (if come) does not change this state. The timing pulse resets the initial state thus preparing the gate to the next operation period. This reset switching induces at the gate output a similar voltage pulse presenting the logic unity. Such pulse does not arise in the absence of the signal pulses S_i so that the OR function is really performed.

Figure 3a shows a possible structure of the NOT gate which is typically a bottleneck in all Josephson junction logics. The gate consists of the interferometer similar to discussed above accompanied by the buffer stage (J_3, J_4 and R) and the additional conductance G. Josephson junctions J_2 and J_3 form a locked pair similar to Goto pair[14]. The timing pulse triggers the 2π-leap of the phase of one of the junction J_2, J_3 depending on the state of the interferometer. The conductance G and Josephson junction J_3 provide low-impedance ways for signal and timing pulses respectively. As one can get convinced by the simulation results† presented in Fig. 3b, the output pulse arises only if junction J_3 has been switched. Our analysis has shown that the circuit presented in Fig. 3a can also be

† $I_{C1} = I_{C2} = I_{C4} = 75$ μAmp; $I_{C3} = 2I_{C1}$; $I_g = 0.75 I_{C1}$; L = 44 pH; M = 53 pH; R = 1 Ω; G = 1 Ω^{-1}; $I_C R = 1$ mV; $\beta_c = 0.7$; RSJ model.

used as a OR-NOT gate, which alone is sufficient to compose an arbitrary logic circuit. It can be convenient, however, to use also other logic gates such as OR (Fig. 2b), AND (Fig. 2c) and some others.

Basic Features of the RSFQ Logic

The RSFQ logic can mean a drastic improvement of the Josephson-junction computing. Firstly, the total time period per a logic operation including the gate reset (see plots in Fig. 3b) can be only factor of 5 to 10 longer than the single Josephson junction pulse time. As the result, the operation frequency of the logic circuits with quite ordinary externally-shunted Josephson junctions (Nb-NbO_x-Pb; $j_c = 10^3$ Amp/cm^2; $S = 10$ μm^2; $\beta_c = 0.7$; $I_cR = 0.3$ mV) can be as high as 30 GHz, i.e., a factor of 10^2 faster than that of the resistive logic. Employing the modern edge-type high-current density junctions[15] with $\beta_c < 1$ without external shunting would allow one to increase the operation frequency by one more order of magnitude. Secondly, the physical similarity of the signal and timing pulses enables one to arrange local generation and logic processing of the timing pulses using the similar logic circuitry. As a result, one can abandon the idea of the clock general for the whole processing device, limiting oneself to the local timing for each fragment. In the same time, presence of the timing pulses makes the mutial synchronization of the computer readily attainable.
Lastly, according to our simulations using the COMPASS program[16] all the circuits discussed have critical current margins as large as at least ±20%[18]. This large tolerance for the parameter scattering gives every hope that basic logic gates operating according the new principle will be realised experementally in the nearest future, so that construction work on the digital devices could be started.

Possible Applications

The RSFQ logic is most suitable for superfast information processing inside a single chip rather than for the interchip communication which should be carried out (at much lower rate) by the usual resistive logic circuits. In order to convert the RSFQ signal to the

resistive logic signal one can employ a hysteretic (high-β_c) Josephson junction stage[7], while the backward conversion can be carried out, for example, using a hysteretic (high-ℓ) single-junction interferometer[5].

The first type of digital devices which could benefit from the superfast RSFQ logic family is the micro-conveyer data flow signal processors with the information exchange between the near gate. Such processor can perform, for example, fast Fourier transform or Fermat transform of the input signal.

The second possibility is to use the RSFQ logic to realize the "microprocessor" approach to design of the large universal computers. In this approach the whole device consists of a large number of VLSI circuits of few types. Each microcircuit contains the RSFQ logic circuitry with some T-pulse lines controlled by some lower-rate (say, resistive) memory cells; contents of these cells determines function performed by the microcircuit. The large loss of the operation rate, typical for this hardware-saving approach, can be made unsubstantional due to extremely high speed of the RSFQ logic.

Lastly, one should note that all the RSFQ circuits are logic flip-flops rather than mere gates. Thus they can be naturally used to design sequential switching circuits, and probably more complex devices with internally-distributed information storage, including associative and "active" memories.

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18. It is important to note that the margins can be increased by some nonvanishing inductance of the junction shunts.