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Superconductive Time-to-Digital Converters

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Abstract—We have designed, fabricated, and successfully tested a superconductive multi-hit Time-to-Digital converter (TDC). The TDC circuit consists of a 30-bit counter, 8x30 first-in-first-out (FIFO) buffer, and a 30-bit parallel-to-serial converter. The value of the counter is latched while the counter is operating at full speed. The successive events (or hits) are accumulated in a FIFO buffer based on RSFQ shift registers. We present details of our TDC designs and their testing at low and high speed.

I. Introduction

HYPRES has been pursuing several digital circuits with the best chances for practical applications in the nearest future. We use several criteria to define such circuits. First, the circuit performance specifications must be out of the reach of competing semiconductor circuits. Second, the integrated circuit complexity should be within existing fabrication capabilities. Practically, these circuits should have the complexity in the order of several thousand Josephson junctions (JJs), comfortably available today at HYPRES' low-temperature superconductor (LTS) foundry [1]. Third, the circuit input/output (I/O) requirements should not exceed the level of interface technology available and commercially practical today. And finally, the cryocooling overhead should be acceptable for customers.

One of these circuits is the recently proposed time-to-digital converter (TDC). The initial RSFQ design of the TDC and its successful demonstration has been reported elsewhere [2]. The main application of TDCs is the high energy physics (HEP) instrumentation with hundreds of thousands of channels per system. The HEP instrumentation performance requirements are extremely high. The CERN' Large Hadron Collider (LHC) detectors require technical solutions exceeding the capabilities of modern semiconductor electronics.

Low power dissipation of the TDC circuits and their ability to resolve multiple time events with high time resolution (a multi-hit time resolution) put the RSFQ TDCs far beyond the capabilities of their semiconductor counterparts. The low power dissipation (~ 0.5 mW per TDC channel) allows the integration of cooled front-end detectors with TDCs inside the detector cryostats. This dramatically simplifies the interface between detectors and readout electronics by eliminating the performance bottleneck of such systems [2]. None of the high-time-resolution semiconductor TDCs can resolve multiple events with high time resolution. Currently, one can obtain either slow multi-hit TDCs or high-time resolution single hit circuits. The RSFQ TDCs provide both high time resolution and high multi-hit time resolution. This is a new opportunity for HEP detector systems designers allowing the reduction of the multiple-year duration of HEP experiments.

The integrated circuit complexity of the RSFQ TDC is well within the current capabilities of commercial HYPRES LTS circuit fabrication. The simple single-hit TDC employs just about 500 JJs per channel [2]. It allows us to integrate a number of channels per chip and still produce it with reasonable yield.

The I/O requirements for the RSFQ TDC are simple since they rely on serial output. The output digital word is serialized using an on-chip parallel-to-serial converter. The single wire per each TDC is used to deliver digital data to room-temperature electronics. The bandwidth requirements (i.e. the wire heat load) is much lower compared to that required for analog event pulse transmission.

Cryocooling by liquid helium is widely accepted in HEP community primarily due to the use of superconductor magnets. The detectors based on Visible Light Photon Counters (VLPC) are also used at helium temperatures [3].

In this paper, we report on further progress in the development of the RSFQ TDCs. We present the design and test results of the first multi-hit TDCs based on RSFQ binary counters and shift registers.

II. Design and Layout

A. TDC Design

The design of this RSFQ TDC takes advantage of the ability of RSFQ binary counters to operate at very high clock frequencies. It allows us to perform a time digitization by direct counting of high-speed clock pulses. Consequently, the TDC time resolution is equal to a clock period.

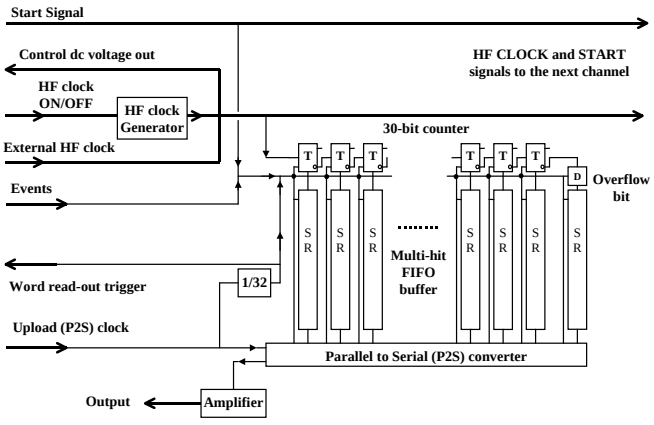

Fig. 1. Block diagram of a single channel of multi-hit TDC.

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Fig. 1 shows a block diagram of the RSFQ multi-hit TDC circuit. It consists of a binary DRO counter, first-in/ first-out (FIFO) buffer, and a parallel-to-serial converter. Several dc/SFQ converters are used to convert the external high-speed counter clock, upload clock, event and start signals into an SFQ form. The high-speed clock is constantly applied to the counter. The START signal resets the counter to zero by performing its destructive readout. The high-speed clock is also applied to the synchronizer. This circuit synchronizes the asynchronous event pulses generated by the input pulse detector. Each event causes a destructive readout process in a counter and a shift of data in FIFO buffer by one word.

In order to minimize the number of output lines, we use a parallel-to-serial (P2S) converter based on B flip-flop cells [4], which differs from the parallel-to-serial converter used earlier in [2]. The advantage of this new converter is its ability to sustain the parallel data overflow. This feature is important for the multi-hit TDC designs. Fig. 2 shows schematics of the new parallel-to-serial converter. In contrast to the old P2S converter design, each P2S converter cell has a RESET input. The clock from the FIFO buffer clears P2S converter cells before loading each new word.

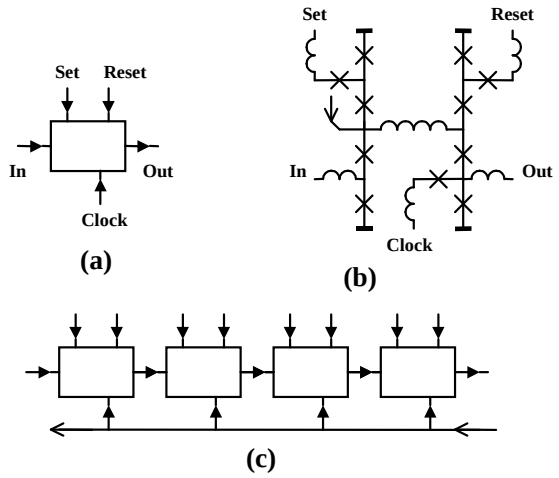

Fig. 2. A novel design of a parallel-to-serial converter: (a) Notation of a single cell. (b) Schematics of a single cell. (c) Block diagram of a parallel-to-serial converter.

The key TDC component is a binary counter with destructive readout (DRO counter). The value of the counter can be read out and reset while the counter is operating at full speed. This is achieved by making the delay in the readout clock line larger than the carry delay of the counter. In this case, racing conditions can not develop. The use of Josephson transmission lines (JTLs) to interconnect the counter stages allows us to set these delays easily.

Thus, the RSFQ TDC possesses virtually no dead time beyond the duration of a single clock period. The circuit is always available for the next counting operation. Therefore, the device multi-hit resolution equals the single-hit time resolution. This feature makes our TDC far superior to semiconductor TDCs, which have a multi-hit resolution much worse then their single-hit time resolution. The readout counter values can be stored into a FIFO register integrated on the same IC. Then the stored data can be read out to external electronics.

Due to a flexible design, multi-channel TDC can work in both COMMON START and COMMON STOP regimes, depending on order of START and EVENT signals.

B. Layout & Chip Design

We have implemented a 30-bit, 8-word multi-hit TDC using a 1.0 kA/cm^2 and 14-bit single-hit TDC using a 2.5 kA/cm^2 HYPRES' standard Niobium processes [2]. Fig. 3 shows the layout of the 30-bit, 8-word multi-hit TDC.

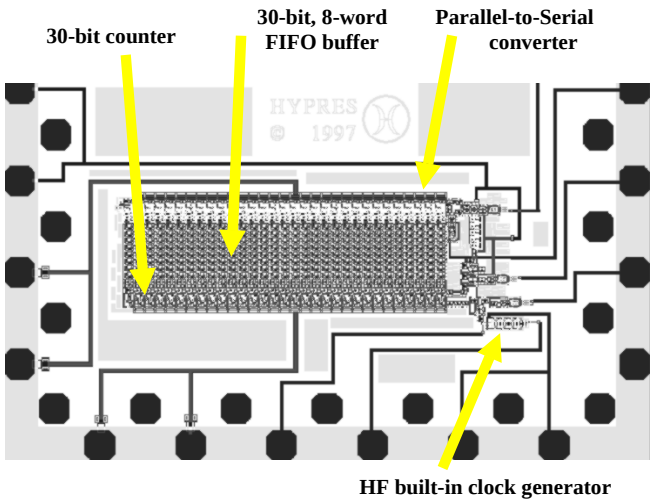

Fig. 3. Layout of a 30-bit, 8-word multi-hit TDC circuit. Chip size is 5mm x 5mm.

For some applications, it is highly desirable to have a few TDC channels on the same IC in order to minimize timing jitter. This allows multiple TDC channels to be perfectly synchronized to the start of an experiment. Due to the low power dissipation of the RSFQ TDC, multiple TDC channels can be implemented on a single IC, ensuring perfect mutual synchronization.

III. Test Results

A. Functionality testing.

Functional testing was carried out at low frequency (about 1 MHz) using conventional pattern generators and oscilloscopes.

Correct and full operation of the 30-bit multi-hit TDC channel has been successfully demonstrated. The measured

dc bias margins for the counter part is ±27% and for the FIFO part is ±13%. Fig. 4 shows an example of correct operation. In this test, we prepared a sequence of 8 events separated by progressively increasing intervals. As Fig. 3 shows, relative time of arrival of all these events have been successfully digitized and captured in a FIFO buffer, and then serially read out.

The first word of eight 30-bit stored words is a random initial contents of counter. All other seven numbers produce roughly a geometric progression with coefficient 2.

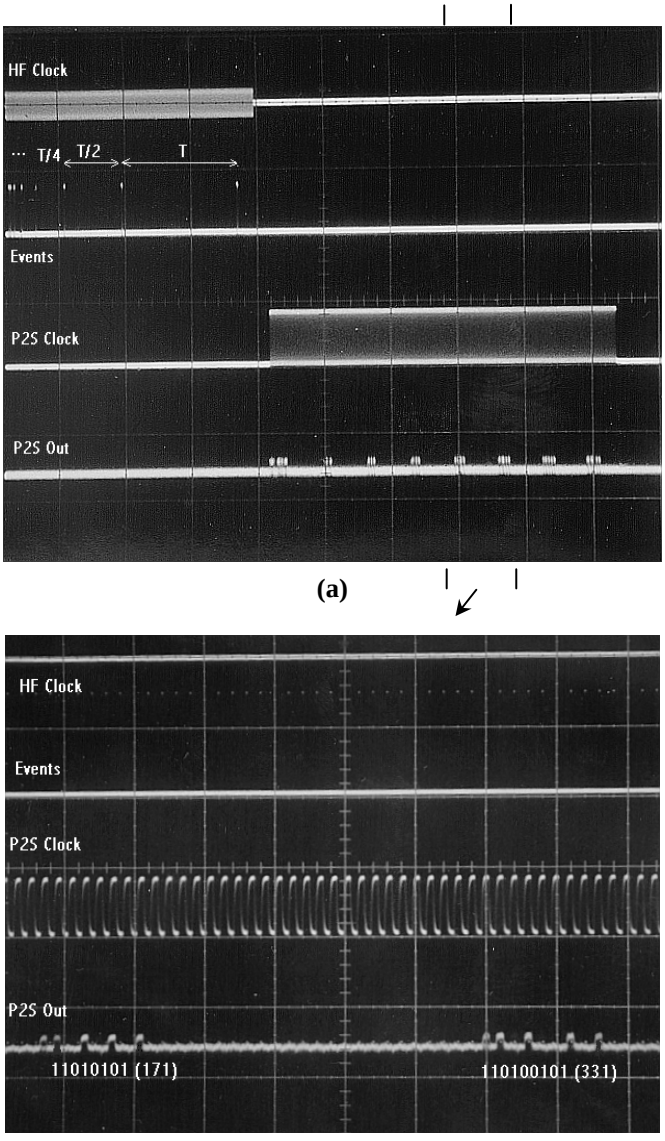

Fig. 3. Successful operation of a 30-bit, 8-word multi-hit TDC. (a) Measurement of the time between successive event pulses. (b) Zoom-in of two successive counts. Traces from top to bottom: HF clock, events, parallel-to-serial converter clock, and output.

B. High-Speed Test.

We have transferred the layout of a 14-bit TDC to a 2.5 kA/cm^2 fabrication process in order to increase speed. The circuit has been fabricated and successfully tested up to 20 GHz clock frequency at ±5% dc bias current margins. The clock was a high-frequency generator, operating in asynchronous regime. Fig. 4 shows correct high-speed TDC operation. In contrast to the previously reported TDC [2], this TDC demonstrated more stable and robust operation at high-speed.

We have successfully demonstrated the principal demonstration of our technical approach – the readout and resetting of the binary counter while it is operating at frequency up to 20 GHz. The high speed measurements were done using HP 33120A generators to produce the EVENT and UPLOAD clocks. The high speed counter clock was generated by a 20 GHz HP 8371A synthesized sinewave generator, limiting our high-speed testing to 20 GHz, but enabling to generate precise frequency signal. The outputs were measured on a sampling scope.

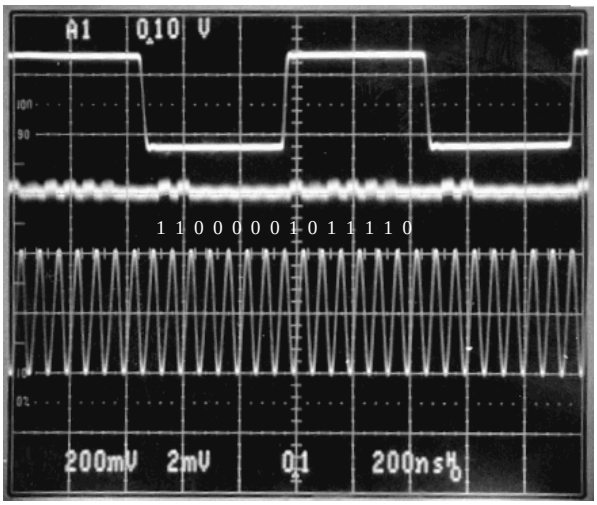

Fig. 4. Correct high-speed operation of a single-channel 14-bit TDC measuring the period between event pulses. Traces from top to bottom are: event signal, output data, and upload clock. The measured time between event pulses is 12,382 clock pulses at reference frequency 12.382 GHz (the event signal frequency was 1 MHz).

IV. Conclusion

The advantage in using superconductive time-to-digital technology lies in its lower power dissipation, higher speed, linearity, and the simplicity compared to semiconductor counterparts. This new superconductive timing circuit will provide a means of insertion of superconducting technology into established silicon technology. Cryocooling issue is greatly simplified for HEP instrumentation applications.

We have designed, fabricated, and successfully demonstrated correct operation of 30-bit, 8-word TDC chips. We have also successfully converted the single-hit 14-bit

TDC for higher critical current density process. The high-speed testing has demonstrated the improved operation at high speed. The demonstrated 50 ps (20 GHz) time resolution has been limited by the test equipment. We have demonstrated the principal task of reading out and resetting a TDC binary counter while it is operating at full speed. We are working on the development of an on-chip stable clock generator to increase the clock frequency up to 100 GHz to attain a 10 ps time resolution.

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