EXPERIMENTAL IMPLEMENTATION OF ANALOG-TO-DIGITAL CONVERTER BASED ON THE REVERSIBLE RIPPLE COUNTER

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Abstract

A new A/D converter which includes a comparator, reversible binary counter with DC outputs has been designed, fabricated and tested. The comparator generates two trains of the SFQ pulses in response to increasing or decreasing of the input signal. The pulses are transferred through SFQ transmission lines to the adding and diminishing inputs of a reversible counter. The reversible counter has been realized by supplementing to the usual counter the SFQ transmission lines, splitters, and confluence elements for sending diminish pulses directly to each bit. Non-destructive read-out of the counter contents is carried out by SFQ/DC converters connected to each counter bit. The integrated circuit is fabricated using 5 μm Nb-AlOx-Nb Josephson-junction technology with critical current density about 500 A/cm^2. External Mo shunts of the junctions provide the value of $\beta_c \leq 1$ and $I_c R \approx 300$ μV. The A/D conversion is studied for low frequency signals with an external clock. High-frequency performance of the reversible counter has been tested by observation of frequency scaling down.

Introduction

Counter-type superconducting A/D converters[1] are very promising for high-accuracy measurements of medium-bandwidth signals. However, at least two evident problems - reversible counting and error-free counter contents reading without interrupting the input signal tracking - should be solved before the practical applications. Several approaches [2,3] have been proposed to solve these problems, however up to now no successful experiments with ripple-counter A/D converters have been reported.

We have found and experimentally realized new solutions of these problems on the basis of recently developed ultrafast RSFQ logic family [4,5]. The design of a reversible counter was based on a usual unidirectional RSFQ binary ripple counter, but some new elements were supplemented to it. As a result, in the case of adding SFQ pulses it is applied to less significant bit (LSB) section of the counter, while in case of diminishing SFQ pulses they are applied to all stages of the counter, providing the complementary binary code representation of (-1).

The second problem was solved by using the asynchronous read-out scheme in our converter; its main idea is the application of SFQ/DC voltage converters [6] to all the stages of the counter. As a result, any change of the counter state is almost immediately converted to a corresponding change of the DC-voltage digital output signals. Timing is introduced by sampling these signals with externally driven comparators of appropriate type (in our preliminary experiments room-temperature comparators were used).

In the report we present the details of the A/D converter construction and layout together with experimental results for the A/D converter and stand-alone reversible counter.

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Circuit design

Figure 1a shows the block-structure of the A/D converter. Comparator produces two SFQ pulse trains which go to two separate transmission lines. When the input signal is increased the SFQ pulses go through the adding transmission line to LSB (BIT0 in Fig.1). In the opposite case of input signal decreasing the SFQ pulses go through the diminishing transmission line which is connected to all the stages. These diminishing pulses decrease by unit the contents of the stages. SFQ/DC converters perform asynchronous nondestructive reading-out of state of each bits. Figure 1b shows the equivalent circuit of fragment of the A/D converter, and Figure 2 - the results of its numerical simulations using the PSCAN program.

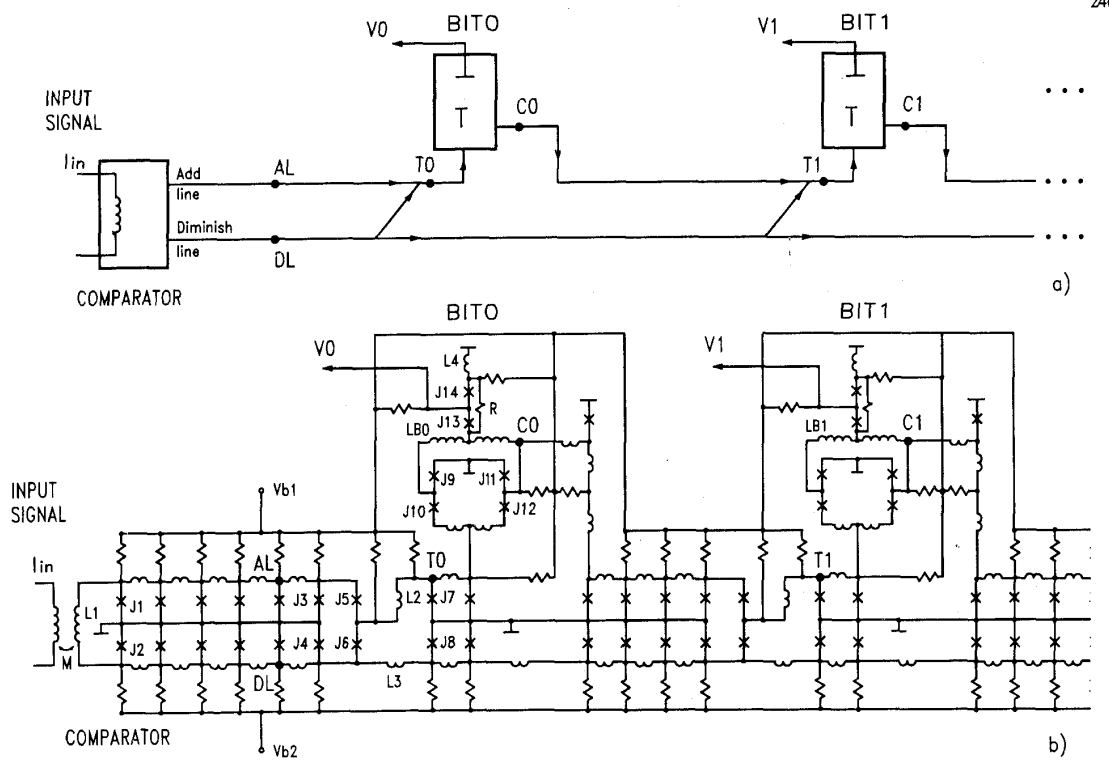
The comparator is the usual two-junction interferometer (J1, L1, J2 in Fig. 1b). The input signal current I_{In} induces a proportional magnetic flux $\Phi = MI_{In}$ applied to the interferometer. If the flux is constant, no SFQ pulses appear at the outputs. If the flux is increased in time, and crosses a level $\Phi_{on} + k\Phi_0$ (with an integer k) the current through junction J1 reaches its critical value and the SFQ pulse is generated by this junction. Thus the SFQ pulse rate at the upper output of the comparator (adding line) equals $|\dot{\Phi}|/\Phi_0$ at $\dot{\Phi}>0$ (see voltage AL in Fig.2). At $\dot{\Phi}<0$, this junction is silent, but junction J2 develops a similar train of the pulses at the reverse output of the converter (see voltage DL).

The split-confluence buffer is a natural combination of split buffer and confluence element[5]. The splitting function is performed by junction J4, inductances L2, L3; confluence function is performed by junctions J3, J4, J5, J6, J7. The parameters of the buffer were defined using PSCAN optimization procedure[7]; the margin of the parameters as high as 30% has been achieved. Simulation showed that proper confluence operation could be realized if the time delay between the input pulses exceeded the pulse duration (about 2 ps for our technology).

T flip-flop with SFQ/DC converter is an optimized version of the element described earlier [6]. Additional inductance L4 is introduced in the circuit for improving parameter margins. Another peculiarity is the application of the bias current to the point between junctions (J11, J12) where the carry output (C0) takes place. As a result the initial state of T flip-flop is "1" providing the zero voltage state of the SFQ/DC converter (V0 = 0). So the initial state of the counter is (111...1) or (-1) in complementary binary code (V0 = V1 = ... = V7 =0).

Figure 2 demonstrates the operation of the first two bits of the A/D converter in case of saw tooth input current I_{In}. One can see that the repetition rates of the SFQ pulses through T0, C0, T1, C1 have the following ratios $f_{T0}:f_{C0}:f_{T1}:f_{C1}=4:2:2:1$ for the adding pulses. Otherwise we have ratios $f_{T0}:f_{C0}:f_{T1}:f_{C1}= 4:2:6:3$ in the case of diminishing pulses.

The drawback of this version of reversible binary ripple counter is the losses of the SFQ pulses in case of



collision adding or carry pulses with the diminishing one in confluence elements. To prevent these events the time delay of the diminishing line is smaller than the delay of the adding/carry line. It results in increasing the delay between carry and diminishing pulses during their passing towards the most significant bit. Moreover, the inevitable time delay sets a certain connection between the quantity of counter bits and frequency of quantization f_r. In the worst case the next diminishing pulse would collide with the previous carry pulse in n-th confluence element, where $n=1+1/(f_r t_{min})$. For 8-bit counter (n=8), and t_{min} = 2 ps maximum f_r = 70 GHz. This frequency exceeds the cutoff frequency of the SFQ/DC converter determined by LBO/R time constant (in our experiment F_{off} = 60 GHz).

Layout Design

We have fabricated our test circuits using the all-refractory 5μ design rule technology [6]. This structure contains four superconducting layers: the ground plane, the base electrode, counter pre-electrode and counter electrode. The layout differs in several aspects from the traditional Josephson Nb-AlO_x-Nb technology. Firstly, the layout included holes in the ground plane intended for pinning of the parasitic Abricosov vortices and filtering picosecond SFQ pulses in interconnecting lines. Secondly, to increase reliability and to reduce the relief steps we have employed two insulator layers which are produced with different pattern. Besides that we try to avoid the crossing of a two conducting bottom layers under counter electrode.

The employed technology is similar to the described in Reference [6]. The Nb ground plane was sputtered on Si substrate with protecting Al_2O_3 layer. The geometry of the ground plane was defined by RIE, all subsequent layers were formed by lift-off. Superconductor Nb films were deposited by DC magnetron sputtering, all insulator SiO layers are thermally evaporated. After formation windows on SiO layer the surface of the bottom superconductor electrode was

Figure 1. Counter-type analog-to-digital converter: block diagram (a); equivalent circuit of its two bits (b).

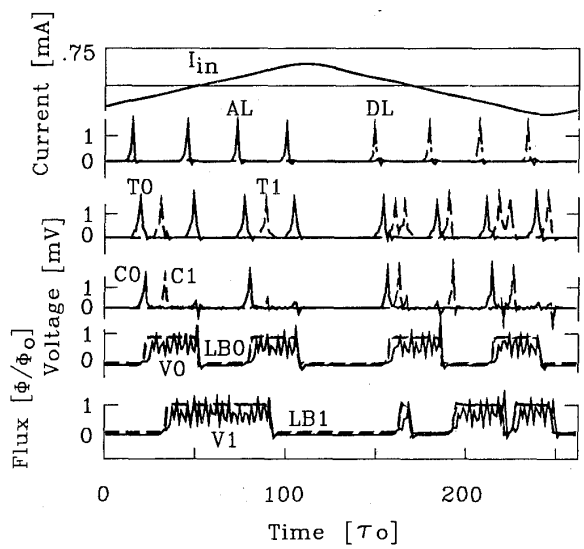


Figure 3. Results of numerical simulation of the circuit shown in Fig.1b for experimental parameter values: $I_{C1} = I_{C2} = 1/2\ I_{C3} = 1/2\ I_{C4} = 2/3\ I_{C5} = 2/3\ I_{C6} = 1/2\ I_{C7} = 1/2\ I_{C8} = 1/2\ I_{C9} = 1/2\ I_{C11} = 2/3\ I_{C10} = 2/3\ I_{C12} = I_{C13} = I_{C14}$ = 0.125 mA, L1 = 2 L2 = 2.4 L3 = 12 L4 = 16 pH, V_C = 0.3 mV, β_c = 1, τ_0 = 3 ps, R = 0.2 Ohm.

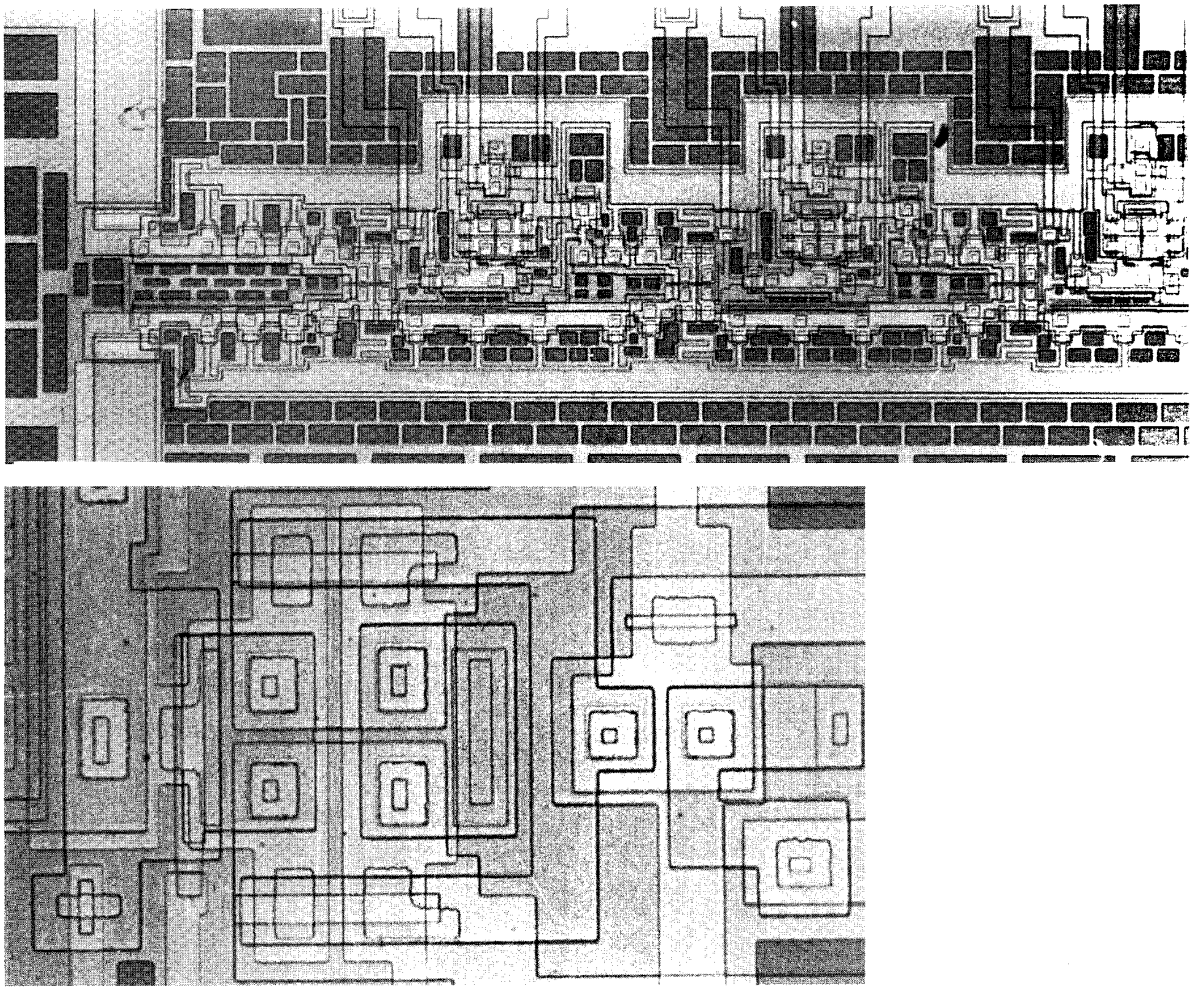


Figure 2. Microphotographs of 8-bit A/D converter chip.

cleaned by RF etching and a thin Al layer (7-10nm) was deposited by RF sputtering. The Al film was thermally oxidized and Nb counter pre-electrode was sputtered in the same vacuum run. This pre-electrode covered only the small regions near the junctions areas. After RF sputter cleaning the counter electrode was sputtered to connect all parts of the integrated circuit.

Three kinds of integrated circuits have been fabricated and investigated. The first circuit was two-bit reversible binary counter with independent adding and diminishing inputs. This independence was achieved by the elimination comparator inductance L1, and the introduction of external currents for biasing of the junctions J1, J2 (see Fig. 1). There were separate current controls of magnetic flux in both T-flip-flop storage interferometers and split-confluences buffers. It was possible to adjust independently power supplies of the adding/carry and diminishing transmission lines for the correction of time delays. The second circuit was two-bit A/D converters which is very similar to described above reversible binary counter but with closed comparator inductance L1. On the base of these elements the eight-bit A/D converter have been designed and fabricated. This integrated circuit contained 169 Josephson junctions and 300 resistors. Limited quantity of the contact pads (16 double pads) allowed to arrange only two (common for all bits) adjustments: currents for the tuning bias of the split-confluence buffers and the magnetic flux in the storage interferometers.

Experimental Results

All measurements were carried out in the temperature range 4.2-6.0 K; the exact temperature value could be chosen to provide the nominal value of the critical current density. The most of the biasing currents were supplied trough specially selected resistors from the common DC power line. The magnitude of the common feeding current was chosen to provide the bias currents about 0.7-0.8 of the critical values for transmission line junctions. To set the correct operation of the T flip-flop we controlled the currents which were applied to the inductances LB0, LB1. In the case of correct operation, the magnitude of the currents through LB0, LB1 corresponded to the minimal value of the interferometer critical current.

The high frequency investigations were carried out by the measuring of the average voltage in different point of the circuit; this voltage and the SFQ pulse repetition frequency f_t are connected by well known relation: $f_t = V/\Phi_0$ (see, e.g., ref.[6]). Fig.4a shows the voltages which were measured in different points of circuit when the junction J1 generates pulses at the fixed bias (adding) as function of the current introduced to point C1 (see fig.1). One can see the step on the output of the counter (C1 curve) at the voltage VC1 = VT01/4 where VT0 is the input voltage. This fact proves the proper operation of the two-bit binary counter. One can see that the step size up to $\mp$ 25% of the current value in the middle of the step is achieved, what

indicates the large enough margins.The voltage after the first stage of the counter (labeled as C0 and T1) is equal to the half of the input voltage T0. In the case of the input current increasing the proper counter operation up to the voltage V(T0)=100μV has been measured, what means that the operation range of the employed SFQ/DC converters lies from zero to 50 GHz.

Fig.4b shows the voltages which were measured in different points of circuit when the junction J2 generates pulses at the fixed bias (diminishing). One can see that the output C1 curve involves the step at the voltage VC1 = 3/4 VT0 which is according to the circuit right operation. The margins value ∓25% is also obtained. In this case the voltage on the first stage output labeled as C0 is equal again the half voltage T0 measured on the input of the counter, while the voltage on input of the second stage - T1 is three times larger then C0 (VT1 = 3/2 VT0) due to the confluence pulses from the diminishing line. The same curves are obtained as function of currents through T1 and C0; the proper counter operation is keeping up to the voltage V(T0) = 90 μV. There is some difference in the adjustment procedure for count-up and count-down. For the diminishing case after the setting input current,we have to adjust one of the power supplies Vb1 or Vb2 in order to correlate the time delays for pulses which are moved in the diminishing and adding/carry lines.

The voltage on the input junctions for both modes of the bidirectional counter operation is larger than the voltage on junctions J1, J2 even if the operation frequency is lower than the upper limit of SFQ/DC converter. It might be caused by the nonuniformity of the SFQ pulse generation due to fluctuation of the external currents. In this case the surplus of generated pulses are buffered by the junctions J5, J6.

The low frequency measurements are carried out for two-bit and eight-bit counters. The triangular current I_{in} was applied to the input (see Fig.5). By changing the offset and amplitude of this current it is possible to set the various regimes of analog/digital conversion. The successful

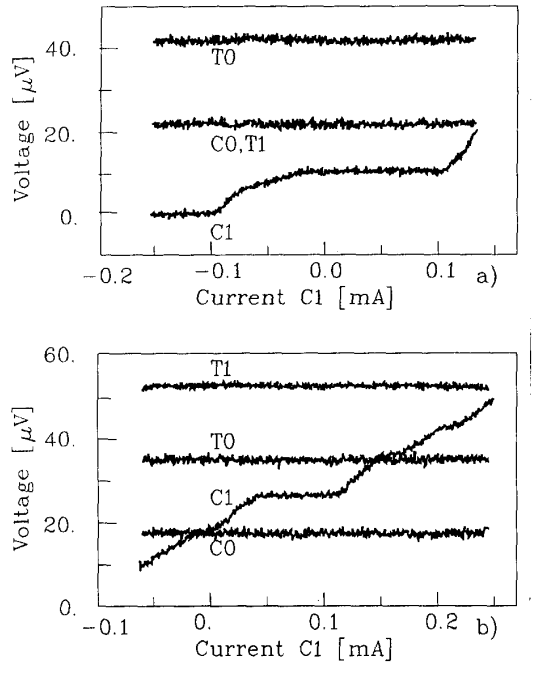


Figure 4. Experimentally measured DC voltages of two-bit reversible binary counter on the inputs T0, T1 and on the carry outputs C0, C1 of BIT0, BIT1 as function of current applied to C1 for regimes of adding (a), diminishing (b) .

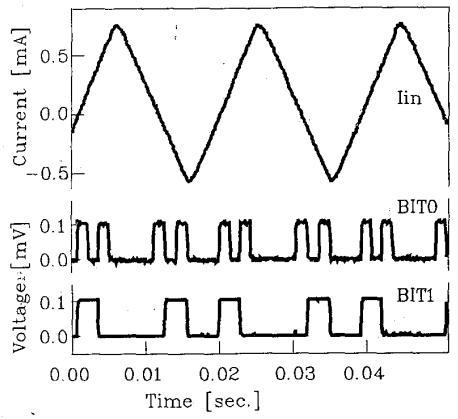


Figure 5. Measured digital outputs V0, V1 of two-bit A/D converter in response of input signal current Iin.

operation of two-bit A/D converter at various parameters of the input signal has been demonstrated. The example of the correct operation where the comparator generates the four pulses both for increasing and decreasing parts of the input signal is demonstrated in Fig.5. One can see a good agreement between the computer simulations and experimental results.

The investigation of the 8-bit A/D converter comprising 169 Josephson junctions and 300 resistors is in progress but the preliminary results show the correct operation for all the bits.

Conclusion

That is the first implementation of Josephson counter-type A/D converter which is very promising for high-accuracy measurement of medium-bandwidth signal. It became possible due to two main achievements: the realization of reversible binary counter and error-free reading out of counter without interrupting signal tracking. As a result, two-bit reversible binary counter with non-destructive SFQ/DC reading out and two-bit analog-to-digital converter have been designed, fabricated and successfully tested.The investigation of the 8-bit A/D converters is underway but preliminary results prove the possibility to create a new type of the SFQ devices with outstanding parameters.

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