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New Elements of the RSFQ Logic/Memory Family (Part I)

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EXTENDED ABSTRACTS

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New Elements of the RSFQ Logic/Memory Family (Part 1)

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Abstract Some new RSFQ (Rapid Single Flux Quantum) logic/memory elements operating at large (up to 100 GHz) frequencies are proposed. In this report new elements (new 2-input AND, N-input AND, half-adder, corrector for A/D converter (Rylov 1990), and branch-off) are presented.

1. Introduction

It is evident now that RSFQ-based logical elements work at very high clock frequencies (Koshelets et al 1987, Kaplunenko et al 1989). Nowadays it is actual to look for the best parameters of existing RSFQ elements providing wider operation range and also to create new elements performing different given functions. One of the peculiarities of the RSFQ logic is that some rather complex elements, e.g., full adders can be designed as indivisible units . This fact essentially extends the set of elementary logic functions. In this paper some new realizations of an AND cell, a synchronising corrector and a directed branch-off are proposed. The gates have been examined with the help of the Personal Superconductor Circuit ANalyzer (PSCAN)(Polonsky, Semenov, and Shevchenko 1991) using the standard RSJ model of a Josephson junction. In all the figures Φ_0 is the value of a single flux quantum, V_c is the characteristic voltage of a Josephson junction and τ_0 is the time unit equal to $\Phi_0/2\pi V_c$.

2. New AND element

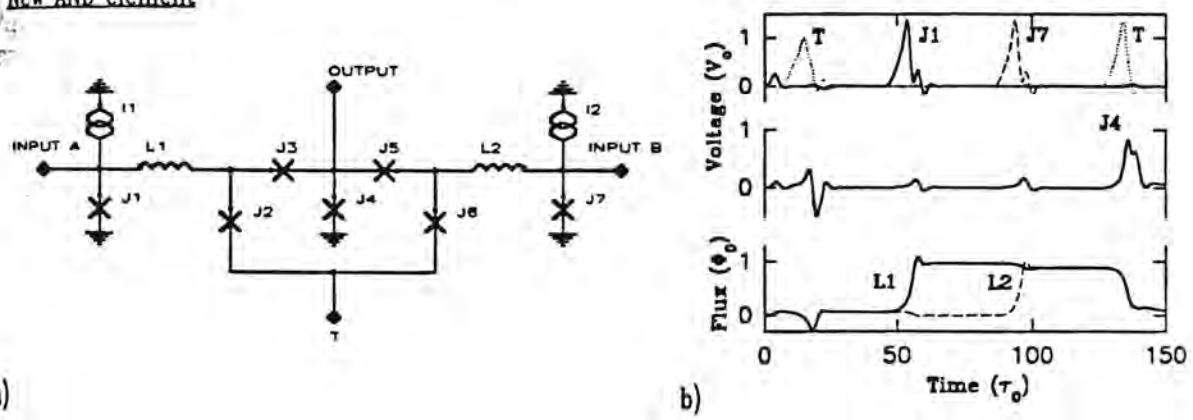

Fig. 1. The equivalent circuit of the AND gate (a) and results of its simulation (b).

The cell shown in Fig.1 performs the AND function. It comprises two storage interferometers: J1, L1, J3, J4 and J7,L2, J5, J4. If no pulse arrives at input terminals A , B then each interferometer is in its "0" state, and while the clock pulse T switches junctions J2 and J6 with no effect on the output (junction J4). If only one input pulse arrives during the clock period (say at input A) it switches the left interferometer to its "1" state, and J6 and J3 (rather then J2 and J4) are switched by the clock pulse, thus the output pulse is not produced. When the both input pulses arrive during the clock period and bias currents of the interferometers branch to junction J4, clock pulse switches only this junction while other junctions remain uneffected.

3. N-input AND element

All the AND cells proposed until now (the cell discussed above and (Mukhanov, Polonsky, and Semenov 1990)) are very difficult to implement with N inputs (N>2). Fig.2a shows the new element which we propose to circumvent this limitation. It is an array of elementary cells shown on Fig.2b.

This cell is an ordinary SFQ flip-flop. The only difference is the addition of junctions J2, J3 which allow one to implement the RESET of flip-flop without changing the state of output junction J5. The SET and RESET pulses arrive at terminals 1 and 2 respectively. Even if the state of the interferometer is "1" and bias current is diverted

to the path L1, J3, J5 the arrived RESET pulse switches the junction J3 instead of J5. The READ pulse arrives at terminal 3. If the state of a cell is "0" then this pulse switches junction J4 and no output pulse is produced. In opposite state the pulse switches J5 producing the output pulse on terminal 4 (OUT).

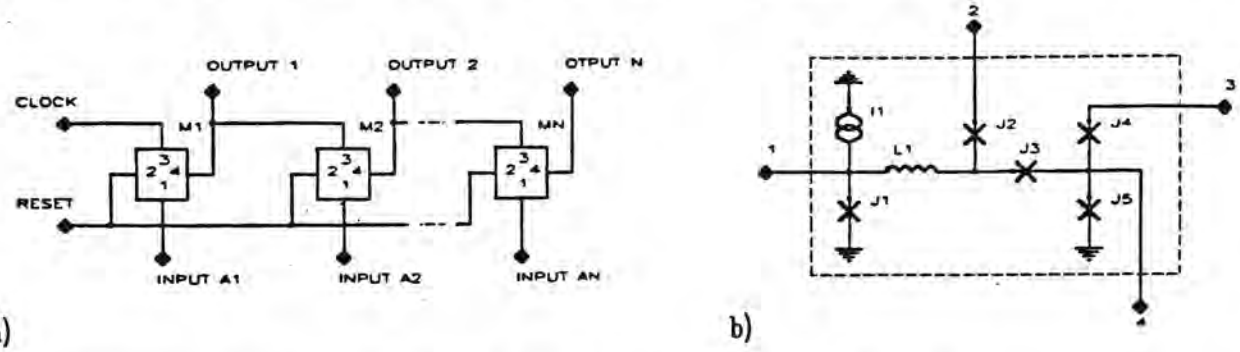

Fig. 2. The equivalent circuit of the N-input AND gate (a) and its elementary cell (b).

The whole N-input AND element operates as follows. During the clock period the input pulses A1, A2.....AN arrive at SET terminals of elementary cells. The clock pulse T arrives at the input READ terminal of the first cell. If the state of this cell is "1", the pulse is reproduced at the terminal OUT and arrives at the READ terminal of the second cell and so on. Thus "1" arise on output of the N-th cell after the clock pulse only if there was "1" in all cells before. One could note that this element produces also partial production A1*A2*...*Ai at the i-th (i < N) output terminal. This property can be employed, for example, in high-speed carry circuitry used in a parallel adder.

4. Half-adder

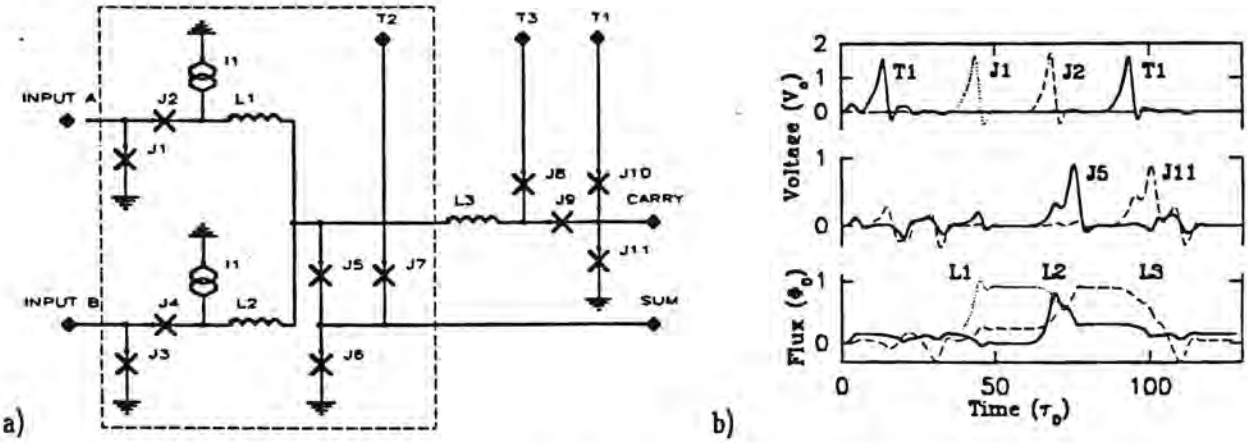

Fig. 3. The equivalent circuit of the half-adder (a) and results of its simulation (b).

In order to implement a parallel adder one needs a half-adder. Possible implementation of this circuit is shown in Fig.3a. To produce the SUM we use the XOR element described in (Mukhanov, Polonsky, and Semenov 1990). Here we only consider how the CARRY is computed. The half-adder is composed of XOR cell (in dashed line box) and additional storage interferometer J5, J6, L3, J9, J11. Clock pulses sequentially arrive at the inputs T1, T2, T3 with small time delays. As in ordinary XOR the junction J5 switches when both input pulses A, B arrive during one clock period. The switch of J5 writes "1" into additional interferometer. This "1" will be read and sent to output CARRY by the pulse arriving at terminal T1. If the state of XOR cell is "01" or "10" then the state of the additional interferometer is "0" and the clock pulse T1 switches J10, and the pulse T2 switches J6 producing output SUM equal to "1". At this moment the state of the additional interferometer becomes "1". In order to reset this state the pulse T3 switches J9 (rather then J8) and the half-adder finishes its clock period.

5. Corrector

The function of the corrector shown in Fig. 5a is to improve matching between asynchronous and synchronous parts of the differential-code A/D converter (see Fig.4a)(Rylov 1990). It synchronizes and corrects asynchronous data pulses coming from the input interferometer and produces output pulse when the clock pulse arrives.

On the one hand the corrector is a two-junction interferometer with a destructive read-out and on the other hand a ternary flip-off-flop (Chan and Van Duzer 1978). It has two inputs S1 and S2 corresponding to the increment and decrement outputs of the input interferometer, the two outputs Q1 and Q2, and the clock input T. The device has three states (with clockwise or counter-clockwise direction of persistent current and with zero current). When a pulse from any input terminal (either S1 or S2) comes (see Fig. 5b, also 4b) it switches the junction J7 (J8) and is then stored in the interferometer having biased the junction J13 (J9). Note that the next input pulse is ignored in the case when it comes from the same input as the previous one (it switches the junctions J3 (J6)). The clock pulse T gets into the circuit through the junction J11 and then switches the more biased junction (either J9 or J13).

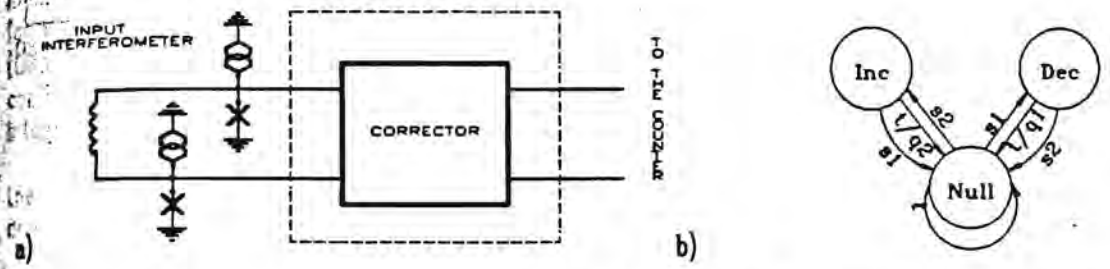

Fig. 4. The block-scheme of the differential-code A/D converter (a) .The left pick-up coil is linked galvanically with some external circuit to be examined. Moore diagram of the corrector (b). The NULL marks the initial state.

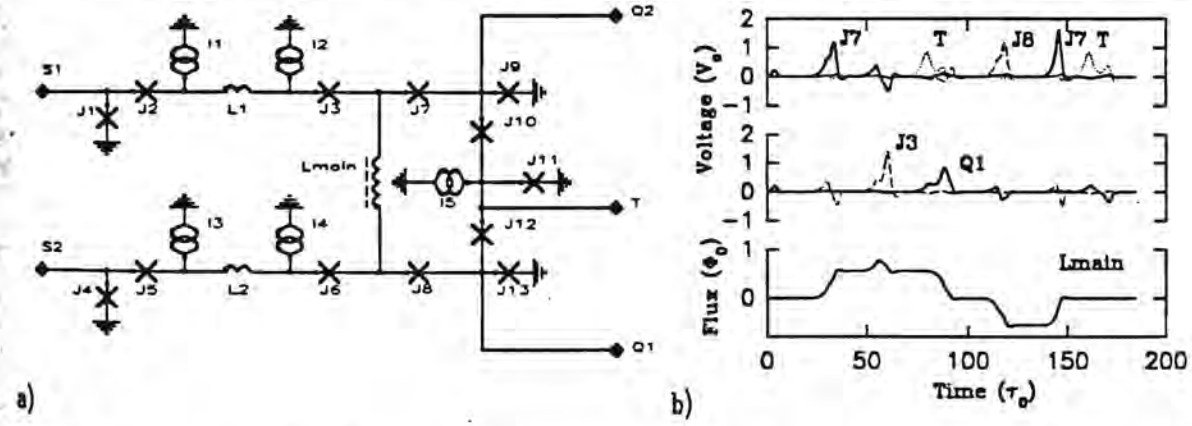

Fig. 5. The schematics (a) and operating diagrams of corrector (b).

If the both data pulses come within one tact period, the device performs the XOR function in order to prevent the counter of sequentially adding and subtracting a unit (correction). The J12 and J10 junctions switch because of their smaller critical currents than the ones of the J9, J13. The buffer stages J1, J2 and J5, J6 are to protect the inputs from the output pulses. To maintain the synchronization and to discard the situation when the two input pulses come simultaneously (the behaviour of the device in such case is undefined) it is useful to link the corrector, the counter and the input interferometer with the help of shift registers (Mukhanov, Polonsky, and Semenov 1990), instead of conventional transmission lines.

6. Branch-off

The directed branch-off shown in Fig.6 gives an opportunity to separate the output and input data streams, for example, in managing data bus . The input and output circuits are linked galvanically (via J5, L1) and inductively (via the transformer T1). When the "def" pulse passes the junction J5 is to switch because of its smaller

critical current so nothing gets into the output circuit, and the original pulse passes the branch-off staying unchangeable. The "through"-pulse induces current in the circuit J4, J6. The J4 junction being overbiased switches to the resistive state. The current flowing through the junction J6 increases that makes J6 also switch and produce the output signal, just as the original pulse is detracted by the buffer stage J2,J3. The galvanic link increases the device performing range and accelerates the process of switching. The device is asynchronous, which fact allows us use it both in tacted and non-tacted schemes.

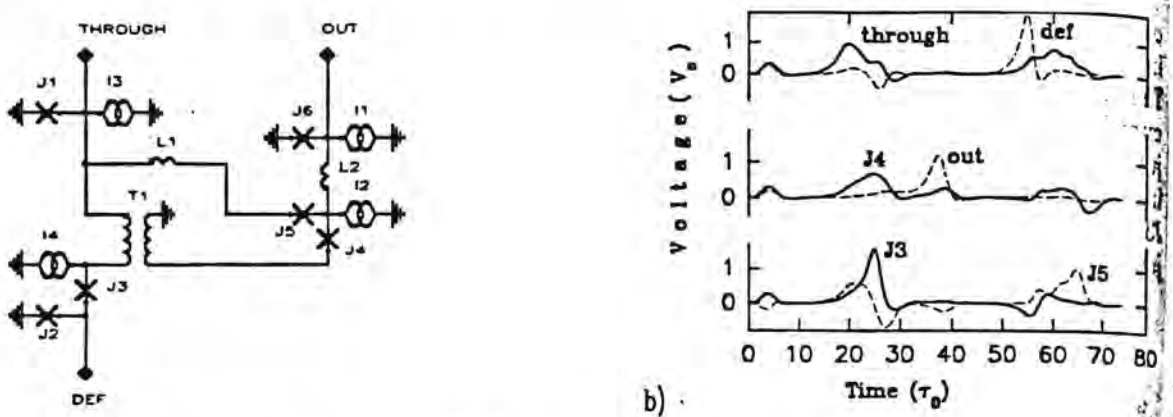

Fig. 6. The schematics (a) and operating diagrams (b) of the branch-off.

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