Progress in the Development of a Superconductive High-Resolution ADC

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Abstract—This paper is a progress report on the development of a high-resolution analog-to-digital converter (ADC) which uses a phase modulation/demodulation architecture. Presented are an analysis of the performance limitations, proposed design improvements, and recent test results. Test results for new versions of room temperature VXI-based interface and processing modules are also described.

I. Introduction

Recently, we reported the first full implementation and high-speed performance evaluation of our high-resolution superconductive ADC, which uses a phase modulation-demodulation technique [1]. This initial demonstrated ADC performance was competitive with the best reported semiconductor ADCs to date. However, the performance was considerably lower than projected. In order to identify reasons for this discrepancy and ways to improve the ADC, we have conducted further tests and performed a systematic ADC design analysis and revision.

II. ADC System

We have expanded our superconductive ADC concept to include a cryogenic/room-temperature interface (Fig. 1) with semiconductor post-processing to facilitate additional selectable decimation filtering to achieve dynamic programmability of ADC resolution and bandwidth. This hybrid scheme allows us to reduce the complexity (i.e. junction count) of the superconductive ADC chip while enhancing the overall ADC performance and versatility.

III. ADC Front-End Design Analysis

The most critical part of the ADC system is the ADC front-end (Fig. 2). This block consists of a clock generator (ac/SFQ Converter) producing an SFQ (single flux quantum) clock from an external sinewave and a modulator/ demodulator performing an analog-to-digital conversion using a phase (time-delay) modulation technique. The modulator/demodulator comprises a reference phase generator (RPG), a quantizer, and a race arbiter (or synchronizer).

A. Reference Phase Generator

The accuracy of the ADC cannot exceed the accuracy of the reference phase, which is modulated by the measured signal. In previous papers [1-3] the RPG had not been discussed; it was presented simply as an ideal source of dc voltage exactly corresponding to one half of the clock frequency. In accordance with the fundamental Josephson relationship between voltage and phase, the RPG produces a linearly growing phase.

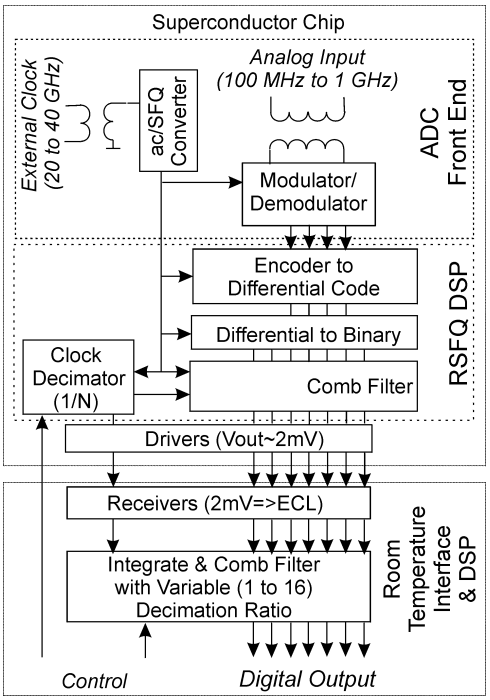

Fig. 1. Block diagram of the new-generation ADC system combining a superconductive ADC chip with room-temperature post-processing.

A basic element of the RPG is a delay line, which is implemented using a Josephson Transmission Line (JTL) with an additional output tap (Fig. 3). These elements are connected sequentially, while the taps are connected with the generator output **R** via equal inductances *L1,…Lm* (Fig. 2). This produces packets with a fixed number (*m*) of voltage pulses per packet, or an *m*-step staircase of the phase as shown in Fig. 4.

Each SFQ pulse passing through the delay lines produces 2π phase steps on the taps. The output of RPG (point **R** in Fig. 2a) produces a staircase-shaped phase φ_R with smaller step sizes to make the height of all *m* steps equal to 2π. The growth of φ_R leads to a growth in current I_q. However, each time I_q exceeds the critical current I_c of junction J1 (Fig. 2), the current drops down to its initial value I_c-ΔI (Fig. 4b).

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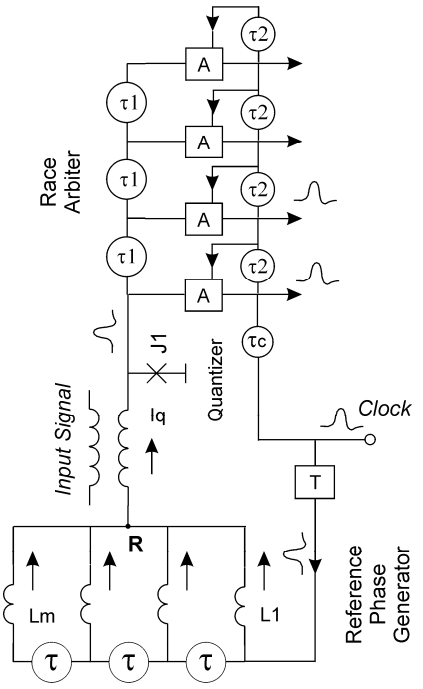

Fig. 2. General structure of the ADC front-end.

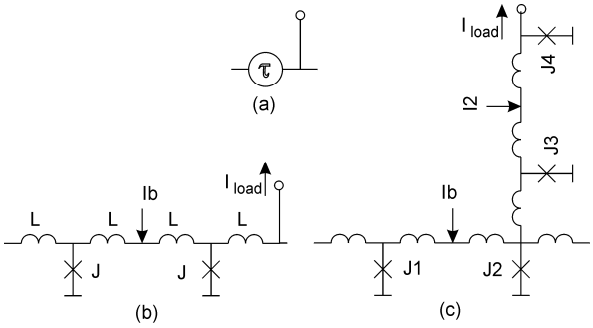

Fig. 3. Delay line for SFQ pulses: (a) notation; (b) the simplest implementation using a section of JTL; (c) an advanced implementation with reduced influence of load current I_{load} on propagation delay.

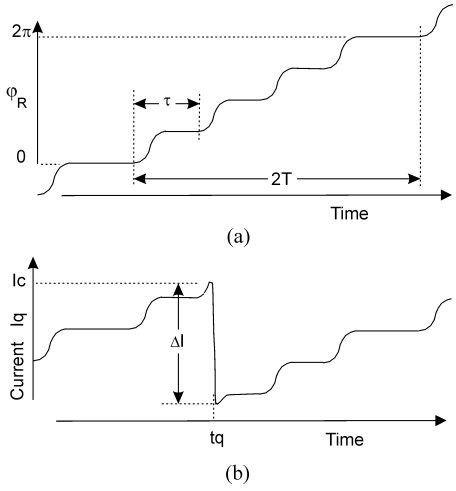

Fig. 4. Operation of the Reference Phase Generator (RPG): (a) RPG produces multi-step staircases of phase; (b) however switching of junction J1 keeps current Iq (c) within margins ΔI.

B. Modulation/Demodulation

The input signal (current) modulates current *Iq* and, as a result, shifts switching time t_q (Fig. 4b). This time shift (or delay) can be detected in a race arbiter by using a set of similar delay lines and clocked comparators (arbiters) **A** (see top of Fig. 2). The delay in these lines (τ1) is slightly higher than in the generator to compensate for the clock skew τ2 between arbiters: τ1=τ+τ2. For proper operation of the ADC, the delay τc is adjusted to provide that the lower half of the arbiters generate SFQ pulses "1" in the absence of an input signal.

C. ADC Performance Factors

The modulation/demodulation ADC described above has a particularly unique feature—the digitization of a dc signal is insensitive to variations of the clock frequency. Indeed, a variation of the clock period does not change the local (within a clock period) moments of the switching of junctions in the RPG and quantizer; however, the circuit is sensitive to other factors, which can influence circuit timing (delays) and affect the ADC performance.

Factor 1: Individual circuit delays depend on their corresponding bias currents I_b (Fig. 3b). This effect can be used to increase performance by manual delay adjustment, but can also reduce the operating margins due to the introduction of external noise in the bias current. The sensitivity to such deviations could be reduced if all circuitry were fed with a single power line. Currently, we are using many independent power lines to afford the greatest insight during testing.

Factor 2: These delays also depend on load currents I_{load} (Fig. 3). This effect is more difficult to eliminate than Factor 1, because these currents depend on the input signal itself. In particular, the delays are decreased after each switching event of junction J1. This effect can be alleviated if the load current is not allowed to flow via the main delay line, but rather is buffered using additional junctions (J3 and J4 in Fig. 3c).

Factor 3: Circuit delays also depend on the time intervals between successive propagating SFQ pulses. This effect is especially important for the delay lines in the race arbiter block, where the time intervals between subsequent SFQ pulses are modulated by the measured signal.

These key factors limit the ADC performance. Factor 1 is responsible for extra time jitter and thus reduces the ADC signal-to-noise ratio (SNR), while Factors 2 and 3 produce nonlinear distortions and therefore reduce the ADC's Spur Free Dynamic Range (SFDR). Substantial modifications of the ADC front-end design addressing all of these factors are in progress. To verify some of our conclusions, we have made several initial design modifications of the ADC chip reported in [1]. In particular, we have streamlined and simplified the clock and signal paths to the race arbiter. These changes were intended to address Factor 3 as described above.

IV. Test Results

We have tested and evaluated the performance of several modified 14-bit ADC designs with 2-channel race arbiters and 1:64 on-chip decimating ratios. The ADC evaluation test setup was identical to that described in [1]. In order to compare the new ADC performance to our previous test results [1], we ran the ADC chip at the same 11.2 GHz clock and output sampling rate of 175 MS/s (1:64) as was described in [1]. Fig. 5 shows a typical measured FFT spectrum yielding the Effective Number of Bits (ENOB), signal to noise and distortion ratio (SINAD), and SFDR. We tested the ADCs using 10 MHz and 50 MHz sinewaves. For the 10 MHz test, we performed additional post-process filtering in software to remove high-frequency components and effectively reduce the output sampling rate to Nyquist (22 MHz). For the 50 MHz test, no additional filtering was done.

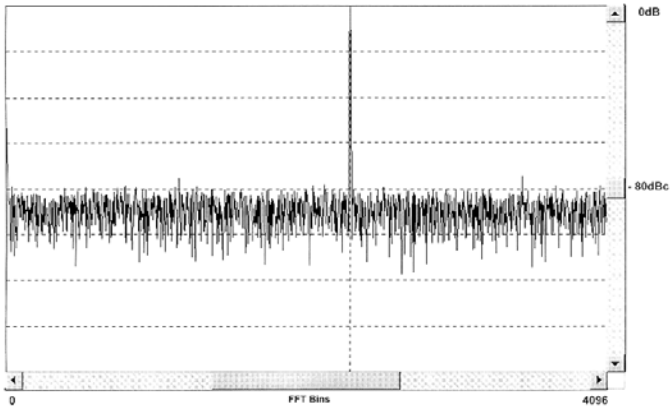

Fig. 5. Measurement of the ADC performance at 175 MS/s (11.2 GHz clock frequency with 1:64 decimation ratio) using an 8K-point FFT spectrum. For 50 MHz input sinewave: ENOB = 8.9 bits, SINAD = 55.3 dB, SFDR = -74.3 dBc (12.3 SFDR bits).

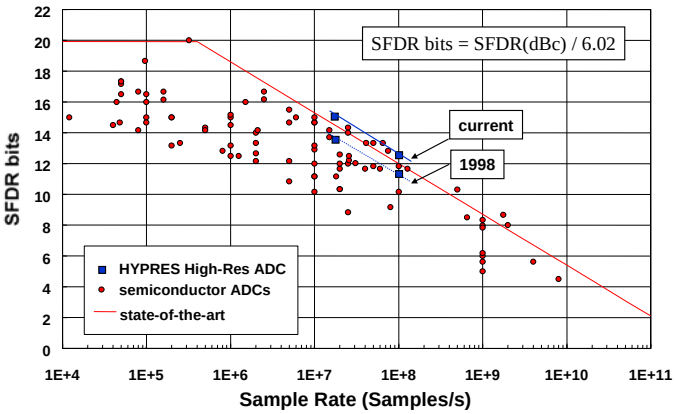

Fig. 6. SFDR bits vs. Sampling rate plot of the ADC performance with our 1998 and current results superimposed. The state-of-the-art semiconductor ADC data are courtesy of B. Walden [4]. The superconductive ADC data are for 14-bit, 2-channel ADC chips operating with an 11.2 GHz clock.

The new results show virtually the same ENOB (SINAD) performance as before: for 10 MHz sinewaves, the measured ENOB of the modified ADC chip achieved the same 12.0 bits at 22 MS/s as the previous ADC design. However, the SFDR performance improved noticeably: -89.7 dBc compared to -80.6 dBc previously. In the case of 50 MHz sinewaves, we observed a similar trend. The ENOB for the 50 MHz tests remained virtually the same (increasing from 8.8 to 8.9 bits) while the SFDR improved from -68.6 dBc to -74.3 dBc. These results are consistent with our theoretical conclusions described in section III.C (Factor 3).

The revised ADC design demonstrates stable operation up to a 12.0 GHz clock rate; however, the measured SFDR at this clock rate was somewhat lower (by about 9 dB) than that at 11.2 GHz. At a 12.8 GHz clock rate, the amount of digital errors (glitches) became too high to conduct further ADC performance evaluation.

Fig. 6 shows an ADC performance plot (SFDR bits vs. Sample Rate) for state-of-the-art semiconductor ADCs as compiled by B. Walden [4]. Our previous [1] and current ADC data are superimposed for comparison. As a direct result of our ADC design modifications, our recent SFDR results now surpass the best reported semiconductor ADC performance to date.

V. Room Temperature Interface and DSP

As shown in Fig. 1, the new generation room-temperature section of our ADC system consists of receiver modules to amplify and convert the ADC chip outputs to ECL levels and a DSP (digital signal processor) module to provide additional decimation filtering with a user-programmable oversampling ratio. The 200 MHz receivers were implemented using a VXI environment to improve shielding, grounding, and power supply, compared to our previous interface implementation using regular VME-bus [1].

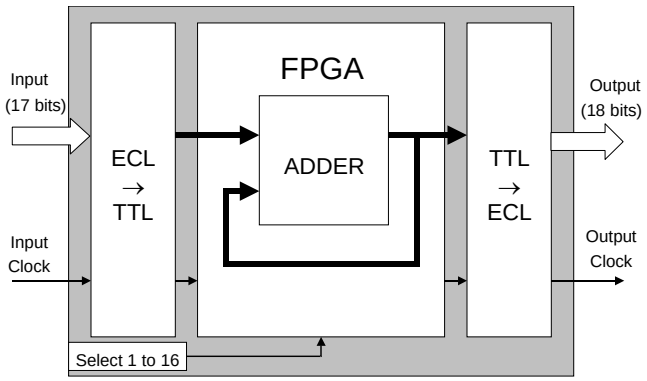

Fig. 7. Block diagram of the DSP module - an integrate and comb filter with a variable 1 to 16 oversampling ratio.

The DSP module performs an integrate and comb filter function, with user-selectable oversampling ratio. It is implemented using a C-size VXI module and has a 17-bit differential ECL data input, an 18-bit differential ECL data output, as well as a clock input and a clock output. Every time a clock signal is received, the data present at the input are added to the content of an accumulator. After a pre-selected number of samples have been added, the output of the module is updated with the sum of these numbers, an

output clock signal is generated, and the accumulator is cleared. The number of samples to be combined is selected via a front panel switch in the range 1-16.

Fig. 7 shows a block diagram of the DSP module. The accumulator and the output clock generator are implemented in a Xilinx XC4003E Field Programmable Gate Array (FPGA). Since the FPGA uses TTL signal levels, the inputs and outputs of the module are level shifted in ECL → TTL and TTL → ECL converters. The current version of the DSP module can operate at an input clock frequency of 80 MS/s limited by the FPGA speed. The next version of the DSP module is being designed to operate at up to 400 MS/s.

Table I shows a summary of the testing of the room-temperature interface including the DSP module at f = 80 MS/s using a 14-bit ADC chip with 1:64 decimation ratio. In order to meet the 80 MS/s limitation, we had to restrict the operation of the ADC chip to a 5.12 GHz clock frequency (64 x 80 MHz). The results obtained show correct operation of the DSP module at different oversampling ratios N: the DSP module produced an ENOB gain corresponding to the expected gain of $\log_2(f / 2\,N\,BW)^{1/2}$, where BW is the signal bandwidth.

Fig. 8 shows a photo of the VXI-based system comprising a clock receiver module, four 4-bit data receiver modules, and the oversampling DSP module. The receiver modules contain additional features such as monitoring outputs of the ADC chip using a regular oscilloscope, etc. A new set interface of modules, which are currently under development, will operate up to 2 GS/s.

Fig. 8. Room temperature VXI receiver and DSP boards. From left to right: clock receiver, four data receivers, and DSP module.

TABLE I

ROOM-TEMPERATURE OVERSAMPLING MODULE

(test results with an ADC chip operating at 80 MS/s, 5.12 GHz internal clock, and 5 MHz input sinewave)

oversampling ratio of the module N	1	2	3	4
average ENOBs	6.21	6.68	6.94	7.15
gain (experiment)	0.00	0.47	0.73	0.94
gain (theory)	0.00	0.50	0.79	1.00
increm. gain (experiment)	0.00	0.47	0.26	0.21
increm. gain (theory)	0.00	0.50	0.29	0.21
error (10 measurements)	0.03	0.08	0.03	0.03

VI. Conclusions

We have identified a number of factors that can limit the performance of our high-resolution ADCs based on the phase modulation/demodulation architecture. The key issues can be attributed to the certain design facets affecting the timing of the front-end section of the ADC system. Our initial, relatively minor, design modifications addressing some of these issues allowed us to improve the ADC linearity. For the first time, the measurement results demonstrated SFDR performance exceeding the best reported semiconductor ADCs. With further design modifications, we expect to exceed the performance of state-of-the-art semiconductor ADCs substantially.

Acknowledgment

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References

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[4] Bob Walden, HRL Laboratories, walden@hrl.com.