Extended Abstracts of 7th INTERNATIONAL SUPERCONDUCTIVE ELECTRONICS CONFERENCE (ISEC'99)
June 21-25, 1999, Berkeley, CA USA

A Superconductive High-Resolution Time-to-Digital Converter

Oleg A. Mukhanov and Alex F. Kirichenko
HYPRES, Inc., 175 Clearbrook Rd., Elmsford, NY 10523, USA

Abstract—We are developing an ultra-high resolution time-to-digital converter (TDC) based on a novel scheme combining a digital "coarse" TDC and analog "fine" TDC. The coarse TDC is derived from a previously reported RSFQ time digitizer based on binary counters. The fine TDC is based on an analog prescaler. A 31 GHz counter defines the coarse (~32 ps) time resolution, while the prescaler provides a fine time resolution by measuring time within a clock period with 4 ps resolution.

I. Introduction

We have been developing RSFQ (Rapid Single Flux Quantum) time-to-digital converters (TDCs) based on binary counters [1-3]. While these TDCs provide exceptional multi-hit time resolution, ultimately, their time resolution is limited to the level of a single clock period. Therefore, any increase in TDC performance can come only with an increase in the circuit clock frequency. We can project reaching a 12-ps resolution using 80-GHz counters; however, to go beyond the 10-ps mark would require using an enhanced circuit fabrication process.

Recently, a number of applications have been identified which require a sub-10 ps TDC. One of the high-profile applications is the Muon Cooling for the Muon Collider project – a novel particle accelerator concept for high-energy physics. In order to achieve the required TDC time resolution of 6 ps for this application, a novel TDC design must be devised. This TDC must be capable of resolving times shorter than the TDC clock period. This paper presents the design and the first test results of a high-resolution TDC which specifically addresses this challenge.

II. High Resolution TDC Design and Test

A. General Block Diagram

Fig. 1 shows a block-diagram of the proposed high-resolution TDC. The TDC design is based on a combination of our proven all-digital TDC (Coarse TDC) [1-3] and a novel analog prescaler (Fine TDC). The TDC resolution is set by the maximum counter speed divided by the number of channels or bins in the analog prescaler. For instance, a 31 GHz TDC with an 8-bin analog prescaler will be capable of measuring time intervals with 4 ps precision.

The digitized time stamps can be stored in a multi-hit buffer or first-in/first-out (FIFO) register integrated on the same IC. The multi-hit TDC resolution will still be limited by the time resolution of the Coarse TDC. The output of the superconductive TDC will be accessible via a parallel-to-serial converter and room-temperature interface, all run by a control module based on the VXI standard (VMEbus Extensions for Instrumentation).

Manuscript received May 7, 1999.
This work was supported in part by US Department of Energy under contract No. DE-FG02-98ER-82595.

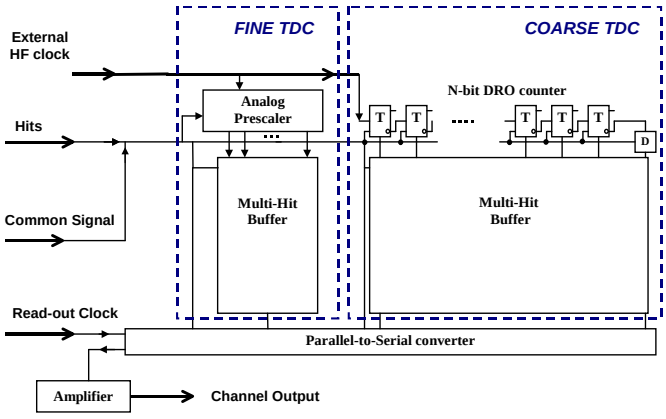


Fig. 1 Block diagram of the single channel high-resolution TDC with Coarse TDC and Fine analog prescaler TDC.

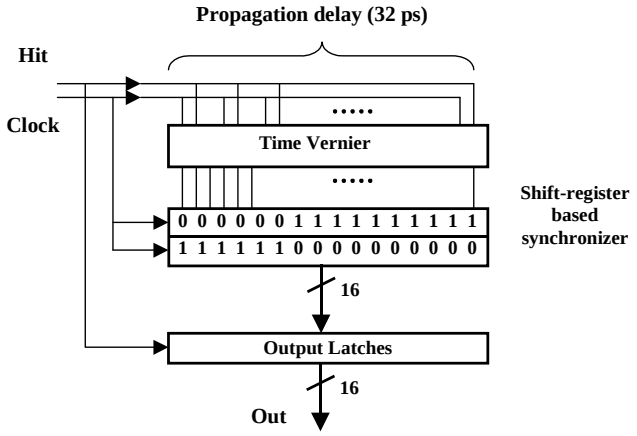


Fig. 2. Block diagram of the analog prescaler (Fine TDC) based on time vernier.

B. Analog Prescaler Based on Time Verniers

Fig. 2 shows a block diagram of the analog prescaler. The design of this circuit is similar to that of a multi-channel race arbiter (or synchronizer) employed in the HYPRES high-resolution ADC [4]. The prescaler consists of two parts: a time vernier and a two-phase synchronizer. The design of the time vernier is based on SFQ pulse propagation along a Josephson Transmission Line (JTL). The velocity of an SFQ pulse strictly depends on the dc bias current applied to the JTL. We exploit this dependence to tune and calibrate the time vernier. To detect the position where the two pulses meet (CLOCK and HIT), we use a series of 8 latches (for an 8-bin prescaler) distributed uniformly along delay lines. The

HIT line is connected to the inputs of these latches, while the CLOCK line triggers the latches and destructively reads out their data. Thus, after every HIT, we have two 8-bit words of ones and zeroes. In the first word a series of "ones" are followed by a series of "zeroes". The number of "ones" determines the position along the JTL, where a CLOCK pulse overrides the HIT pulse. A small logic block picks this first word, converts it into a serial format, and sends it to the output. Using this method, an 8-bin prescaler provides a 4 ps time resolution with a 31.3 GHz clock frequency.

We have designed and fabricated a test prescaler chip using the HYPRES 1.0 kA/cm^2 Nb fabrication process. In order to provide few-ps time delays, we integrated a JTL-based delay line on the same chip. Fig. 3 shows the low-speed test results of this circuit. All output bins were monitored with toggle-type monitors, thus switching of the output voltage state between 0 and ~0.2 mV indicates an output "one" in typical non-return to zero (NRZ) fashion.

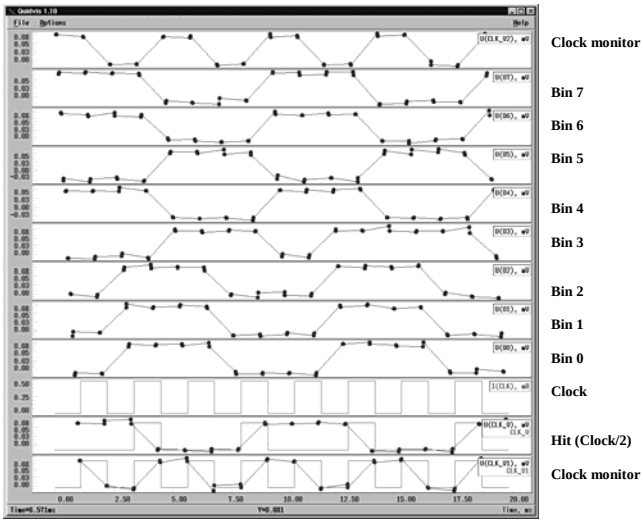


Fig. 3 Correct functionality of the time vernier based prescaler. Total time vernier delay is 50 ps. The preset value of the HIT-CLOCK delay is 20 ps. The output is 1110000, or 3/8 of 50 ps.

The preset value of the variable delay was 20 ps. At the first clock pulse, the outputs of bins 0 through 2 are "one", while the outputs of bins 3 through 7 are "zero". This indicates the delay between CLOCK and HIT pulses is 3/8 of 50 ps (18.75 ps). By changing the dc bias current on the variable delay JTL line, we have observed the expected response on the outputs of the prescaler. A computerized test setup allowed us to measure the operating margins of all critical parameters at different values of the dc bias current for the time vernier. As we mentioned above, the bias current of the time vernier changes the propagation time of the SFQ pulses, thus changing the resolution of the prescaler. In this experiment, we observed our prescaler fully operational at up to 30 ps propagation time, which corresponds to ~4 ps resolution (or 2 ps in case of 16 bins).

Fig. 4 shows the results of a similar experiment performed at a high clock frequency. A picture, taken of an oscilloscope shows the response of all 8 bins of the prescaler with a linear variation of the dc bias current of the variable delay line, i.e. the HIT-CLOCK delay time.

One can see all 8 bins consequently switching to "one", indicating the increase in delay. More importantly, there is no overlapping between bins. This means that internal noise does not affect the resolution of the prescaler at clock frequencies up to 17.5 GHz. We have also achieved successful interleaving above this frequency, with error-value of less than one LSB (least significant bit).

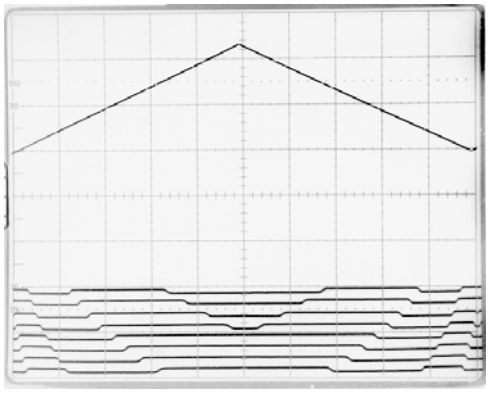


Fig. 4 High-speed operation of an 8-bin analog prescaler based on a time vernier at 17.5 GHz. Upper trace is a current, controlling the delay between CLOCK and HIT signals. Bottom traces are 8 output bins.

We have successfully measured a full transition width of 2 ps from dc to 15 GS/s and of 3 ps at up to 20 GS/s (Fig. 5). These results prove that the prescaler transition width is sharp enough to build a 16-bin prescaler, i.e. to interleave the individual bins without superposition of their transitions.

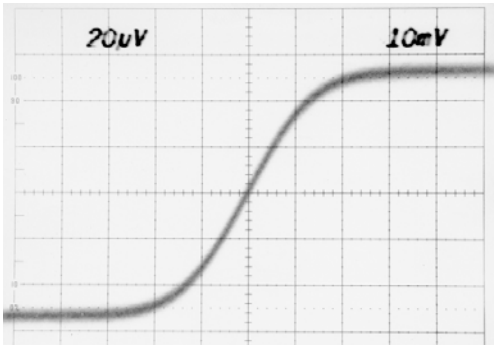


Fig. 5 Measured discrimination curve (1 ps/div).

There are, however, a few drawbacks of the time vernier. It leads to a cumbersome design, sophisticated post-processing electronics, and requires complicated tune-up and calibration processes.

C. Analog Prescaler Based on Dynamic AND-Elements

To avoid the drawbacks mentioned above, a novel design for an analog prescaler based on dynamic AND-elements has also been proposed. This novel design will allow us to increase the sharpness of the transitions seen in Fig. 4, enabling us to interleave 16 bins of prescalers. This new design also allows us to substantially simplify the peripheral logic. Fig. 6 shows a schematic of this new prescaler. It is

based on a novel dynamic AND gate. This gate produces an output when the delay between input pulses is less than a particular threshold value.

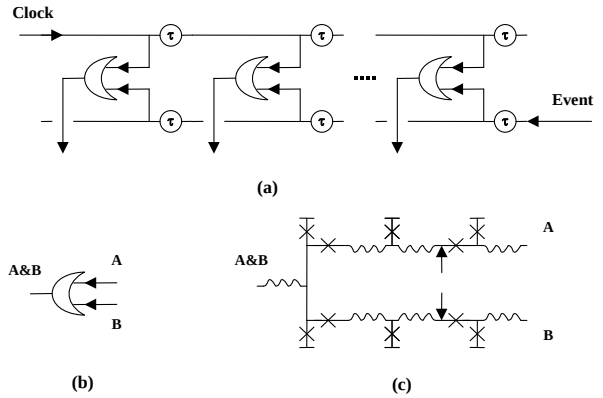
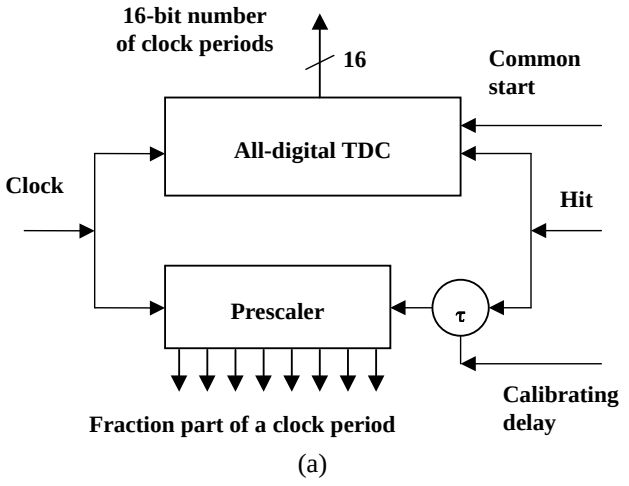


Fig. 6 An analog prescaler based on dynamic AND-elements: (a) block diagram; (b) notation, and (c) schematic of the dynamic AND-element.



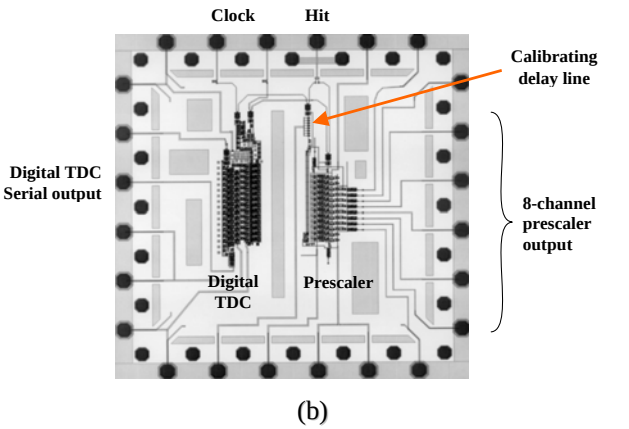


Fig. 7. A 4 ps single-hit TDC using an 8-bin Fine TDC and a 14-bit Coarse TDC: (a) block-diagram and (b) chip layout.

In this design, the CLOCK and HIT pulses are moving toward each other from opposite ends of the two delay lines. These delay lines are connected with dynamic AND gates. The delay between two AND gates (τ) is 2 to 6 ps. The dynamic AND gate has an internal cycle time, which is set to 1.5 τ. If and only if two pulses arrive at the input terminals of the gate within this time interval, the gate will produce an output pulse. In this way, we can detect the position along the delay line where the HIT and CLOCK pulses meet.

The delay element τ is a segment of a Josephson transmission line (JTL). The delay time of this element can be tuned by changing the bias current of the transmission line, allowing one to adjust the prescaler to other clock frequencies. A 16-bin version of this prescaler with a 31 GHz clock frequency will result in a time resolution of ~2 ps.

D. High-Resolution TDC Chip

Fig. 7 shows a block diagram and chip layout of the integrated TDC chip. The TDC consists of two parts, – a digital Coarse TDC (counting clock periods) and an 8-bin Fine TDC (measuring a 1/8 fraction of the clock period). The digital part counts the number of clock periods between COMMON START and HIT signals. The analog part (the 8-bin prescaler) gives the position of HIT pulse corresponding to CLOCK pulse in 1/8's of a clock period. This provides a time resolution of up to 2 ps. Both analog and digital parts share the same CLOCK and HIT terminals. To remove any induced delay between signals arriving at the digital TDC and prescaler, we use a calibrated delay line. The calibration process for this line is simple. By applying the same signal to both CLOCK and HIT terminals, the user sets the reading of the prescaler to exactly zero.

III. Conclusion

We are developing a TDC based on the combination of the fine-resolution analog prescaler and a coarse digital TDC, which will provide a substantial performance improvement over both existing as well as prospective TDCs based on other technologies. We have successfully demonstrated 6 ps performance and have shown the feasibility of 2 ps time resolution.

Acknowledgment

We thank D. Brock, A. Bross, S. Rylov, and J. M. Vogt for helpful discussions and assistance.

References

[1] O. A. Mukhanov, A. F. Kirichenko, and J. M. Vogt, and M. S. Pambianchi, "A superconductive multi-hit time digitizer," *IEEE Trans. Appl. Supercond.*, vol. 9, 1999. (in press).
[2] O. A. Mukhanov and S. R. Rylov, "Time-to-digital converters based on RSFQ digital counters," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 2669-2672, Jun. 1997.
[3]A. F. Kirichenko, O. A. Mukhanov, and S. V. Rylov, "Superconductive time-to-digital converters", in: *Extended Abstracts of ISEC'97*, Berlin, Germany, vol. 1, pp. 34-37, Jun. 1997.
[4] S. V. Rylov, L. A. Bunz, D. V. Gaidarenko, M. A. Fisher, R. P. Robertazzi, and O. A. Mukhanov, "High resolution ADC system," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 2649-2652, Jun. 1997.