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DESIGN AND TEST OF RSFQ FULL ADDERS

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The RSFQ circuits of 1-bit, 2-bit, and 4-bit full adders (FA) for a projected digital filter have been designed, simulated, and successfully tested. The single bit employs 22 Josephson junctions and occupies an area of 230 x 110 μm^2. The maximum clock frequency is 13 GHz for the 2-bit FA. The circuits were experimentally studied with the on-chip Logic Tester and SFQ Sampler. Various performance dependencies were obtained.

DESIGN, SIMULATION, AND LAYOUT. A full adder can be designed as a combination of gates which results in a large and complex circuit [1]. An internal memory and the high switching speed of RSFQ elements (primarily, flip-flops) allows a drastic simplification of a FA design by trading off clock rate for the number of employed junctions. This approach is based on a successive processing of each input pulse using a single toggle flip-flop [2]. To prevent a concurrent arrival of input SFQ pulses, every clock pulse sequentially reads out the contents of all input latches (Fig. 1a) which, in many concrete applications, can be the stages of preceding circuits. The FA bit consists of a 3-to-1 confluence buffer, a T1-element, and a read pulse splitter (Fig. 1b,c). A 3-to-1 confluence buffer provides a fan-in of 3 for the T1-element. The T1-element, a toggle flip-flop with destructive reading out of "1", performs summation and asynchronously produces a CARRY signal. A READ signal produces a synchronous SUM output and resets the flip-flop. The design of the T1-element is based on the bi flip-flop circuit [3]. For an N-bit FA, the clock successively reads out the contents of all bits by traveling along the read splitter network.

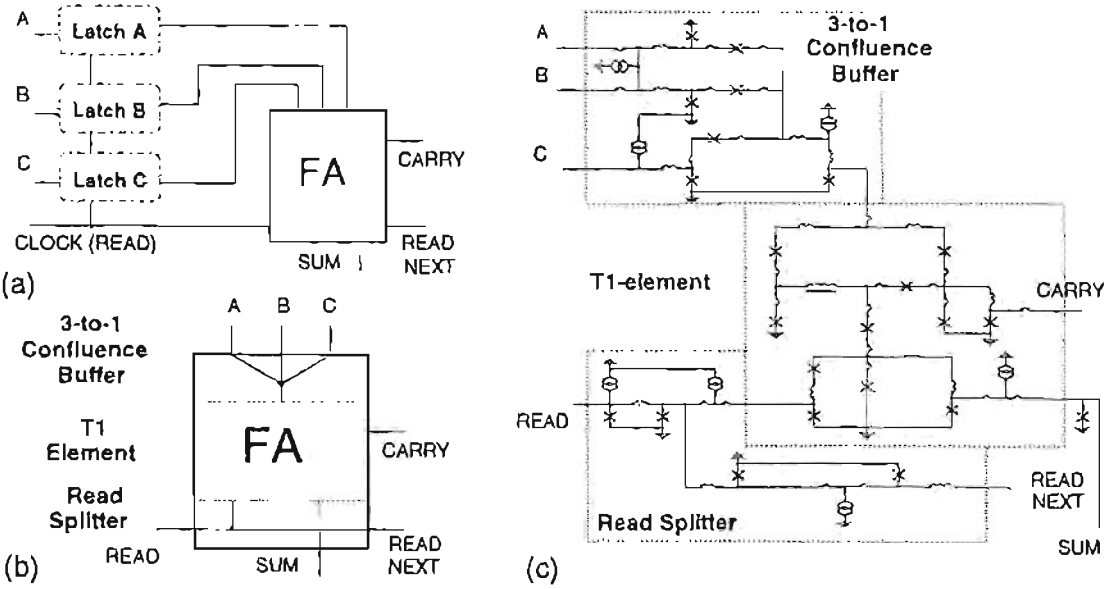

Fig. 1. Single-bit FA. (a). Generic design. (b). Block diagram. (c). Schematic.

A 1-bit FA (Fig. 1c) has been optimized using the PSCAN' optimization procedure [4]. The margins of all circuit parameters including parasitic inductances (51 parameters in total) have been calculated: critical currents > $\pm$30%, inductances > $\pm$44%, dc bias resistors > $\pm$25%, critical current density > $\pm$23%, common dc bias current > $\pm$26%. Three chip types, 1-bit, 2-bit, and 4-bit FAs, have been designed for HYPRES' standard Nb' process with target Jc = 1 kA/cm^2. All FA circuits were inserted into the four channel on-chip RSFQ Logic Tester [4] complemented with an SFQ Sampling Scope.

TEST RESULTS. *Low-Speed Test.* Fig. 2a shows the results of a functional test of a 2-bit FA with Logic Tester. All possible input patterns were applied. The measured margins of the common dc bias are ±20% for 1-bit, ±13% for 2-bit, and ±5% for 4-bit FA, respectively.

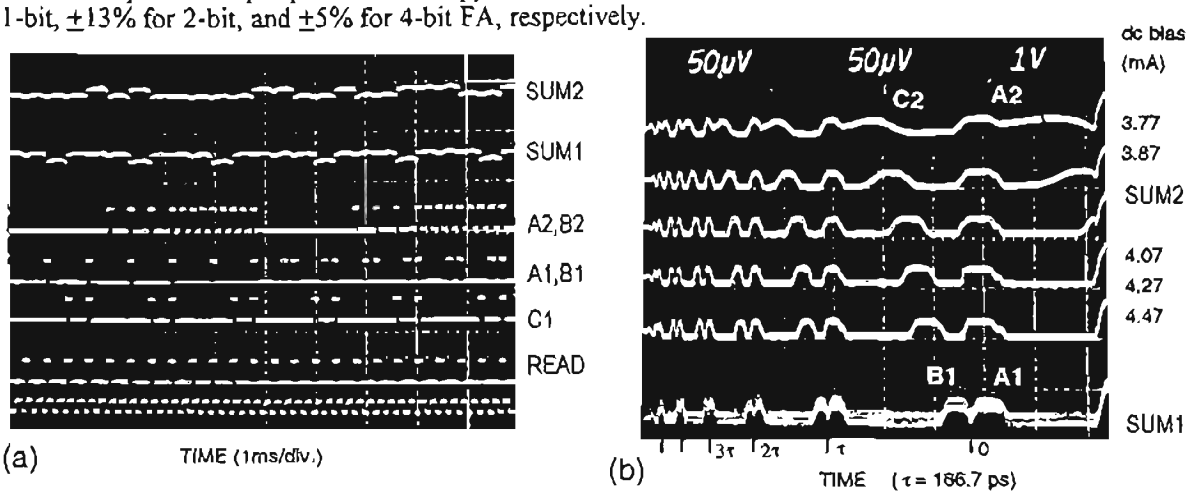

Fig. 3. Test results for a 2-b FA. (a) Low speed operation. Note that all FA outputs are read out by T flip-flop sensors. (b). Measurement of carry pulse (C2) delay vs. circuit dc bias at 6 GHz.

High-Speed Test. The sampling technique has been used for a high-speed test. Each FA bit works as a coincidence detector. Applying a slow sweep current to the bias of the read signal delay line, we monitor the dc voltages across the FA outputs, a procedure which performs a natural averaging of the samples. The low time jitter (< 0.5 ps) is preserved by having on-chip variable-delay lines for data and read signals which enables calibration with an accuracy of < 0.5 ps. When the scanning read pulse does not coincide with data pulse, the monitored voltage level corresponds to the expected output (0 or 1). When a coincidence with data pulse occurs, the voltage level deviation observed (positive or negative) marks the data pulse location. The technique allows the measurement of the circuit response time, the maximum clock frequency, the switching delay rather than the exact pulse waveforms. Moreover, a detailed investigation of circuit dynamics on the chip allows the localization of features which are design constraints, particularly those responsible for the sharp decrease in the bias margin with number of the FA bits.

The typical result of a circuit dynamics study is shown in Fig. 2b where the carry pulse delay is investigated as a function of a dc bias in a 2-b FA at 6 GHz. Three input pulses are applied: two sequential input pulses arrive at the bit 1 (bottom trace) and produce a carry pulse for the bit 2, to be added with the previously-arrived third input pulse (five top traces). The expected SUM1 and SUM2 outputs are "0" as is observed (see Fig. 2b). The positive dc voltage "pulses" indicate the locations of all four SFQ pulses, including carry. The photo shows that the lower the dc bias the longer the carry delay and the wider the carry pulse. Eventually, carry pulse hits the next cycle data pulse (top trace). This test reveals the carry path design as a major speed/margin constraint of the circuit. The introduction of the interstage carry latch would fix this problem.

A number of other performance parameters have been studied. The measured maximum operational frequency is 13 GHz for a 2-b FA, and 23 GHz for a 1-b FA with only two input pulses, the latter being the configuration for the projected digital filter circuit.

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[1] C. Hamilton and K. Gilbert, IEEE Trans. Appl. Superconductivity, 1, 157 (1991).
[2] O. Mukhanov, V. Semenov, and K. Likharev, IEEE Trans. Magn., 23, 759 (1987).
[3] S. Polonsky, V. Semenov, and A. Kirichenko, submitted to IEEE Trans. Appl. Superconductivity.
[4] S. Polonsky, V. Semenov, P. Bunyk, A. Kirichenko, A. Kidiyarova-Shevchenko, O. Mukhanov, P. Shevchenko, D. Schneider, D. Zinoviev, and K. Likharev, IEEE Trans. Appl. Superconductivity, 3, 2566 (1993).