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RSFQ LSI Technology in HYPRES

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Abstract—**HYPRES has started a new wave of fabrication and design upgrades in order to achieve higher clock rate, higher integration density, larger number of devices per chip, and increased circuit functionality. We have also making a steady progress towards fully modular cryopackaging encompassing multiple temperature stages available in modern 4K cryocoolers. In this report, we will present the latest results concerning progress in fabrication process, circuit design, cryopackaging and system integration.**

I. INTRODUCTION

HYPRES has developed several versions of cryocooled Digital-RF receiver systems capable of delivering performance and system advantages for satellite and datalink communications, signal intelligence and other wireless applications [1]. These wideband Digital-RF systems benefit from high sampling and clock speed available in superconductor analog-to-digital converters and digital circuits. However, further progress is impeded by a relatively low scale (~12,000 Josephson Junctions) of superconductor integrated circuits (ICs), since the majority of practical applications require greater functional complexity. Also, further improvement in performance can be achieved by the increase in sampling and clock speed. All these indicate the necessity to upgrade our fabrication and design capabilities to achieve higher clock rate, higher integration density and number of devices per chip leading to much greater circuit functionality.

Our Digital-RF receivers were cryopackaged using relatively large commercial (Sumitomo) 4K cryocoolers. Many applications require lower **s**ize, **w**eight and **p**ower (SWAP) cryocoolers with low cost cryopackage. HYPRES is involved with various cryocooler companies to develop low-SWAP cryocoolers. We are pursuing the modular packaging approach to ensure the cost reduction and portability of our cryopackaging solutions to different cryocoolers.

II. PROGRESS IN IC FABRICATION

Currently HYPRES is running a commercial 6-in wafer foundry operation with several fabrication processes for digital/mixed-signal circuits (4.5 kA/cm^2, 1.0 kA/cm^2), SQUID and quantum computing circuits (30 A/cm^2), and voltage standard chips (30 A/cm^2). The minimum Josephson junction (JJ) diameter of 1.5 µm determines the maximum speed for complex (~11,000-12,000 JJs) digital circuits of about 32-40 GHz [1]. In order to increase clock speed and complexity of digital and mixed signal LSIs as well as to increase the overall material quality of fabrication process critical for quantum computing, HYPRES has recently started the next major fabrication and design upgrade cycle leading to the development of new generation of superconductor LSI circuits.

The key to this fabrication upgrade cycle is the advanced photolithography capable of reaching the "self-shunted JJ size" of ~0.3 µm. Consequently, we have acquired Cannon EX-4 stepper (Fig. 1) with 0.25 µm feature size to be installed in HYPRES' new high-class clean room in July 2009. This will allow us to increase JJ critical current density and achieve circuit scaling leading to higher performance and complexity while maintaining an appreciable circuit yield.

- **Cannon EX-4 Stepper**
  - Resolution to 0.25um
  - Wafer size: 200mm; 150mm
  - Resolution: ≤ 0.25µm
  - Throughput: ≤ 100wph (200mm); ≥ 120 wph (150mm)
- **Expected Benefits**
  - Higher clock (~160GHz clock for LSI circuits)
  - Scaled down logic cells
  - Scaled down chip area
  - Narrower microstrips
  - Improved tolerances
  - Higher yield
  - Higher performance

Fig. 1. The new HYPRES photolithography: Cannon EX-4 stepper.

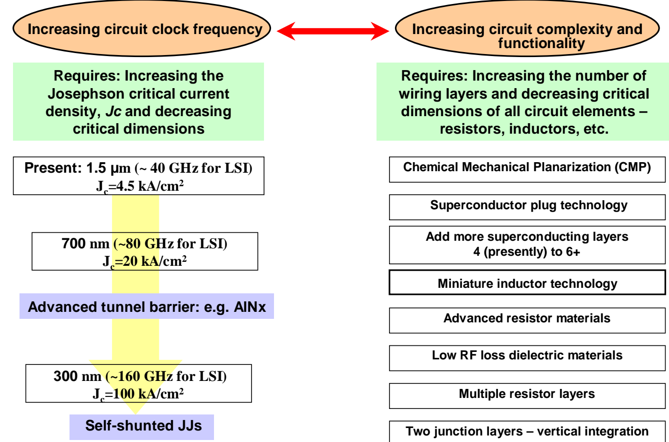

Fig. 2. The planned progression of HYPRES fabrication process. Both LSI circuit speed (clock frequency) and LSI circuit physical and functional complexity will increase.

To ensure quality of high critical current density (high J_c) Josephson junctions, we plan to install a cluster deposition tool (such as KDF). The cluster tool should lead to better uniformity and quality of small high J_c JJs while providing additional flexibility to fabricate JJs with different tunnel barrier materials.

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Fig. 2 shows the planned innovation steps in the development of high Jc, high integration density fabrication process. Currently, we are working on a 20 kA/cm^2 process to achieve ~ 80 GHz clock frequency.

The higher LSI circuit complexity will require planarization in order to add more superconductor wiring levels. This will also require superconductor plug technology with small via sizes. The higher Jc, the higher resistor JJ shunt is required necessitating higher resistivity material. To achieve lower noise and radio frequency (RF) losses, we are acquiring a new dielectric layer deposition tools. We plan to introduce all these innovations in a spiral fashion, so we can always have working foundry. Eventually, all these steps would result in a 100 kA/cm^2 process with two active JJ layers and multiple wiring layers capable of producing 160 GHz high integration density chips.

III. Progress in IC Design

In order to take advantage of the described above new fabrication capabilities, the circuit cell library must be changed. Fig. 3 show an example of immediate advantage in the circuit cell area when better lithography is used. Even greater compactness will be achieved at a functional block level (multiple gate level) once more wiring levels will be enabled by the planarization. Our initial goal is to add 2 more Nb layers at the bottom of the integrated circuits.

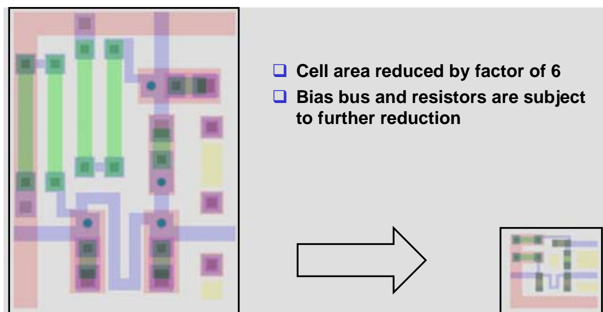

Fig. 3. RSFQ cell scaling achieved for 20 kA/cm^2 process by better lithography. Further cell compactness will be obtained with new wiring layers and reduction of inductance sizes.

IV. Progress in Cryopackaging

We configure our systems following the hybrid-temperature hybrid-technology (ht^2) approach [1] of integrating different functional blocks co-located at different temperature stages and implemented with different technologies. In our recent ht^2 system implementations, the cryopackage has been upgraded to permit replaceable 4K cryomodules housing different chips depending on application. Fig. 4 shows our cryocooled test-bed which can accommodate variety of chips. Recently, we have used the same system to demonstrate the Digital-RF receiver based on a 1-cm^2 ADR chip and the L-band dehopping receiver based on a 5-mm^2 ADC/deserializer chip. Both these chips used similar 4K cryomodules. The system could be reconfigured from the ADR signal acquisition to the L-band datalink by a simple swapping these cryomodules. The cryocooler, wiring, associated rack-mounted equipment remains unchanged. This, although limited, modularization allowed reduction of the system cost.

HYPRES subcontracted Lockheed Martin to produce the first version of a 4K pulse-tube compact cryocooler. It was successfully tested at HYPRES with an RSFQ test chip operating at 46 GHz (Fig. 5). This first cryocooler was driven by a collection of general purpose equipment (generator, amplifiers, etc.). Recently, another cryocooler company Creare has completed a prototype of cryocooler control electronics to drive the Lockheed Martin cryocooler. Further improvements will include even smaller compressor compared to the one shown in Fig. 5.

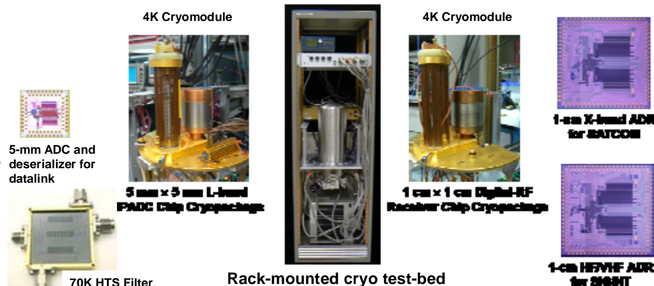

Fig. 4. The Sumitomo-based cryocooled test-bed housing variety of RSFQ chips cryopackaged in the similar 4K cryomodules. The system allows reconfiguration for different applications by changing the 4K cryomodules with different RSFQ chips. The HTS analog filters can be added to a 70K stage if necessary.

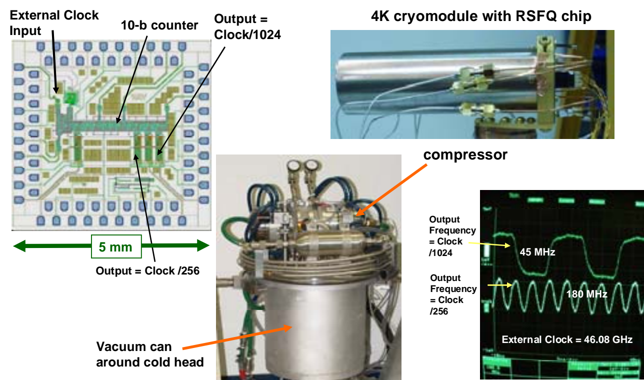

Fig. 5. Lockheed Martin compact pulse-tube cryocooler and an RSFQ test chip mounted on the 4K stage using similar 4K cryomodules of Fig. 4.

V. Conclusion

HYPRES is undergoing a very significant fabrication and design upgrade leading to the development of new generation of superconductor LSI circuits. Our goal is to increase clock speed and complexity of digital and mixed signal LSIs as well as to increase the overall material quality of fabrication process.

Innovations in modular cryopackaging and compact cryocooler development are pursued for reduce overall system size, weight, power and cost.

Acknowledgment

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References

[1] O. A. Mukhanov, D. Kirichenko, I. V. Vernik, T. V. Filippov, A. Kirichenko, R. Webber, V. Dotsenko, A. Talalaevskii, J. C. Tang, A. Sahu, P. Shevchenko, R. Miller, S. Kaplan, S. Sarwana, and D. Gupta, “Superconductor Digital-RF receiver systems,” *IEICE Trans. Electron.*, vol. E91-C, No. 3, pp. 306-317, Mar. 2008.